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Document PER-7
Title ..... Enterprise 64/128 Motherboard Bus
Issue 8
Date ..... 15th August 1985

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This specification is to be used for modules which are required to be attached to the Enterprise expansion motherboard. It details the signals which will be produced on the motherboard edge connectors with the specified loadings, and the loads required to be driven by the expansion modules. These loads and timings will not be the same for a device which is to be attached directly to the Enterprise expansion bus without the use of the motherboard. Any device which will be required to be used in both system configurations must meet both sets of load and timing details.

Buffer ICs used in the motherboard are mainly ALS types to keep added signal delays to an absolute minimum, and to keep the load on the computer edge connector as light as possible. All signals from the computer to expansion modules are buffered with the exception of the picture synchronisation pulses, which are not edge critical and can already drive 10 LS loads. With the exception of the data bus, signals into the computer are not buffered.

The following load specifications are the maximum that may be presented by any single expansion module so as not to overload the motherboard bus with six modules fitted.

All output logic signals give a maximum low level of 0.4 volts and a minumum high level of 2.4 volts into the specified maximum load. All input logic signals require the same levels to be provided by external circuitry. Termination resistors are used on all buffer outputs to keep electrical noise to a minimum.

Signals prefixed '/' are active low. All other signals are active high.

Circuit operation:

U1-5 buffer the CPU data bus, address bus and control outputs in addition to the 8MHz and 4MHz (PHI) clocks. The 14MHz clock, /VSYNC and /HSYNC are unbuffered and only go to slot 1. All buffered lines are provided with termination resistors at the far end of the expansion bus, as the long tracks can cause significant ringing. LED's D1 and D2 indicate that power is applied to the motherboard and computer respectively. The motherboard is powered from an internal triple-output switch-mode supply (transformer is external).

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On power up the operating system examines memory on 16k boundaries to see if RAM is present. Any RAM fitted externally must be decoded down to the 16K level. If it is allowed to echo across any further address space it will be seen by the operating system as being larger than it really is. External ROM's must start on a 256K boundary to be detected by the operating system, but echoing across the unused portion of this 256K space is allowed. I/O space below 80 hex may be used by expansion modules. The motherboard allocates 512k bytes of memory space and 16 bytes of I/O space to each expansion module by the use of three slot-address pins which are hard-wired high or low according to the slot position. These levels must compare with the highest relevant address lines (memory A19-A21, I/O A4-A6) to select the module.

SLOT	MEMORY ADDRESS	I/O ADDRESS
1	080000H-0FFFFFH	10H-1FH
2	100000H-17FFFFH	20H-2FH
3	180000H-1FFFFFH	30H-3FH
4	200000H-27FFFFH	40H-4FH
5	280000H-2FFFFFH	50H-5FH
6	300000H-37FFFFH	60H-6FH

Memory addresses 000000H-07FFFFH and 380000H-3FFFFFH are reserved for use by the main computer. I/O addresses 80H-FFH are also reserved for future enhancements, but I/O addresses 00H-0FH and 70H-7FH may be used by expansion modules although this is not recommended as different modules using these addresses could cause bus conflict.

View looking down on motherboard expansion module connector.

Note that pins a34,b34 are reserved for possible use as a polarizing position.

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SIGNAL	PIN	DESCRIPTION
D0	a14	Active high bi-directional data bus. Used for data exchanges with external memory or I/O devices. Each line can drive 2 LS loads per module. Expansion modules driving the bus must be capable of meeting timing and logic level requirements while driving 11 LS inputs.
D1	b14	
D2	a15	
D3	b15	
D4	a16	
D5	b16	
D6	a17	
D7	b17	
A0	a10	Active high address bus. Provides the address within a 16K memory segment or A0-A7 provide the address for one of 256 I/O ports. Each line can drive 4 LS loads per module.
A1	b10	
A2	a11	
A3	b11	
A4	a12	
A5	b12	
A6	a13	
A7	b13	
A8	a6	
A9	b6	
A10	a7	
A11	b7	
A12	a8	
A13	b8	
A14	a9	Active high address bus. Provides the memory segment address. Each line can drive 4 LS loads per module. These lines may not be stable as /MREQ goes low.
A15	b9	
A16	b26	
A17	a27	
A18	b27	
A19	a28	
A20	b28	
A21	a29	
/RD	a3	Active low read strobe. Used to gate output buffers of memory or I/O devices onto the data bus. Can drive 4 LS loads per module.
/WR	b2	Active low write strobe. Used to strobe valid data on the bus into external memory or I/O. Can drive 4 LS loads per module.
/MREQ	a5	Active low memory request. Indicates that the address bus holds a valid address for a memory read or write operation. Can drive 4 LS loads per module.
/IORQ	b3	Active low input/output request. Indicates that A0-A7 hold a valid address for an input or output operation. Can drive 4 LS loads per module.

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SIGNAL	PIN	DESCRIPTION
/RFSH	a2	Active low refresh signal. Indicates that A0-A6 of the address bus hold a 7-bit refresh address and that the current /MREQ may be used to do a refresh cycle to all external dynamic memories. Can drive 4 LS loads per module.
/M1	a20	Active low signal indicates that the current machine cycle is the op-code fetch of an instruction execution. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle. Can drive 4 LS loads per module.
/RESET	a18	Active low output. Gives 1ms pulse synchronised to the falling edge of /M1 when reset button pressed or when power first applied to computer. Can drive 4 LS loads per module.
/INT	b18	Active low interrupt input. Must be driven with an open-collector device capable of sinking 2.5mA.
/NMI	b5	Active low non-maskable interrupt input. Must be driven with an open-collector device capable of sinking 2.5mA.
/WAIT	a19	Active low signal indicates that an external device is not ready for a data transfer. Must be driven with an open-collector device capable of sinking 2.5mA.
PHI	a22	Z80A clock signal. Nominally 4MHz, with breaks of up to 1.2us when Z80A accesses Nick chip. This signal should only be used for synchronising external events to the CPU, not as a 4MHz clock. Can drive 4 LS loads per module.
1MHz	a21	1MHz 50% duty cycle clock output. Can drive 4 LS loads per module.
8MHz	a23	8MHz clock output. Can drive 4 LS loads per module.
14MHz	b29	Video dot clock. Varies between 14MHz and 14.25MHz depending on TV colour modulation system. This signal contains frequency jitter at half horizontal line frequency. Can drive 1 LS load per module.

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Bus Timing.
Refer to drg A3PER-1.
(Timings apply with the use of specified components operating at a maximum ambient temperature of 70 degress Celsius.)

SIGNAL	REF	PARAMETER	MIN	MAX
PHI	1	Clock period.	250ns	1500ns
	2	Clock high pulse width.	110ns	1380ns
	3	Clock low pulse width.	110ns	1380ns
A0-A13	4	Low address output delay.		117ns
	5	Low address stable prior to /MREQ (memory cycle).	53ns	
	6	Low address stable prior to /IORQ, /RD or /WR (I/O cycle).	173ns	
	7	Low address stable from /RD,/WR, /IORQ or /MREQ.	68ns	
A14-A21	8	Delay from low address stable to high address stable.		87ns
D0-D7	9	Data output delay.		159ns
	10	Delay to float during write cycle.	Not applicable	
	11	Data setup time, M1 cycle.	26ns	
	12	Data setup time, M2-M5 cycle.	41ns	
	13	Data stable prior to /WR (memory cycle).	71ns	
	14	Data stable prior to /WR (I/O cycle).	-24ns	
	15	Data stable from /WR.	46ns	
	16	Input hold time.	9ns	
/MREQ	17	/MREQ delay from falling edge of clock, /MREQ low.		92ns
	18	/MREQ delay from rising edge of clock, /MREQ high.		92ns
	19	/MREQ delay from falling edge of clock, /MREQ high.		92ns
	20	Pulse width, /MREQ low.	220ns	
	21	Pulse width, /MREQ high.	105ns	
/IORQ	22	/IORQ delay from rising edge of clock, /IORQ low.		82ns
	23	/IORQ delay from falling edge of clock, /IORQ low.		92ns
	24	/IORQ delay from rising edge of clock, /IORQ high.		92ns
	25	/IORQ delay from falling edge of clock, /IORQ high.		92ns

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SIGNAL	REF	PARAMETER	MIN	MAX
/RD	26	/RD delay from rising edge of clock, /RD low.		92ns
	27	/RD delay from falling edge of clock. /RD low.		102ns
	28	/RD delay from rising edge of clock, /RD high.		92ns
	29	/RD delay from falling edge of clock, /RD high.		92ns
/WR	30	/WR delay from rising edge of clock, /WR low.		72ns
	31	/WR delay from falling edge of clock, /WR low.		87ns
	32	/WR delay from falling edge of clock, /WR high.		87ns
	33	Pulse width, /WR low.	220ns	
/M1	34	/M1 delay from rising edge of clock, /M1 low.		107ns
	35	/M1 delay from rising edge of clock, /M1 high.		107ns
/RFSH	36	/RFSH delay from rising edge of clock, /RFSH low.		137ns
	37	/RFSH delay from rising edge of clock, /RFSH high.		127ns
/WAIT	38	/WAIT setup time to falling edge of clock.	80ns	
	39	/WAIT hold time from falling edge of clock.	-3ns	
/INT	40	/INT setup time to rising edge of clock.	90ns	
	41	/INT hold time from rising edge of clock.	-3ns	
/NMI	42	Pulse width, /NMI low.	80ns	
	43	/M1 stable prior to /IORQ (interrupt acknowledge).	553ns	

The above timings assume maximum load on the motherboard, i.e. 6 modules fitted each with maximum input loads.

Note that the Dave chip inserts one wait state into each M1 cycle which adds 250ns to the access time of memory on the motherboard bus, but this may be disabled by software. The Z80A also inserts wait states into I/O accesses and interrupt acknowledge cycles.

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SIGNAL	PIN	DESCRIPTION
-12V	b37	Negative 12 volt +/- 10% supply provided by motherboard. A maximum of 100mA is available to power all six expansion modules. This supply is not provided for modules which connect directly to the computer.
+5V	a4,b4	Positive 5 volt +/- 5% supply provided by motherboard. A maximum of 3.30 amps is available to power all six expansion modules. This supply is not provided for modules which connect directly to the computer.
SA0 SA1 SA2	b35 a36 b36	Slot address inputs. These pins are hard-wired on the motherboard with the binary slot number (left slot = 6, right slot = 1). These inputs should be compared with A19-A21 during memory accesses and compared with A4-A6 during I/O accesses to enable the expansion module. A module connected directly to the computer without the motherboard will have these lines wired as slot 1.
N/C	a34,b34	N/C (may be used for connector polarization).

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SIGNAL	PIN	DESCRIPTION
/HSYNC	a32	Active low horizontal picture sync output. Can drive 1 LS load per module.
/VSYNC	b30	Active low vertical picture sync output. Can drive 1 LS load per module.
EC0 EC1 EC2 EC3	a24 b24 a25 b25	External colour inputs to Nick palette. Driving device must be capable of sinking 8mA. These inputs are only available on slot 1, so only one card can drive these lines.
/EXTC	a26	Active low external colour enable signal. When active, inputs EC0-3 are output to video display through colour palette of Nick chip. See Nick programming description for details of priority. Driving device must be capable of sinking 8mA. This input is only available on slot 1, so only one card can drive this line.
L.H.AUDIO	b1	Left-hand channel audio input. 3V pk-pk. into 1k5 for full output. This input is only available on slot 1, so only one card can drive this line.
R.H.AUDIO	a1	Right-hand channel audio input. 3V pk-pk. into 1k5 for full output. This input is only available on slot 1, so only one card can drive this line.
/EXP	b31	Active low expansion data buffer enable. This line must be pulled low by an open-collector device in any addressed expansion module to enable data buffers on motherboard. Driving device must be capable of sinking 6mA.
GND	b19,b20 b21,b22 b23,a30 a31,b32 a33,b33 a35	Supply return and logic ground (11 pins).
+12V	a37	Positive 12 volt +/- 10% supply provided by motherboard. A maximum of 100mA is available to power all six expansion modules. This supply is not provided for modules which connect directly to the computer.

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