CONFIDENTIAL - INTELLIGENT SOFTWARE & ENTERPRISE COMPUTERS LTD.

Document PER-6
Title ..... Enterprise 64/128 Expansion Bus
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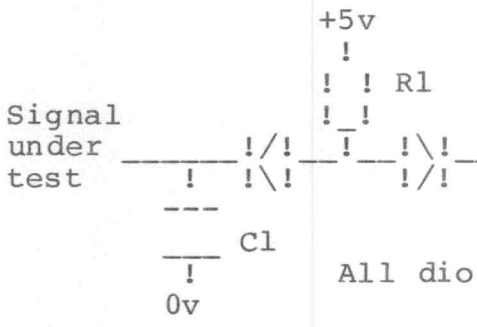
This specification is to be used for modules which are required to be connected directly to the Enterprise expansion bus without use of the expansion motherboard. It details the signals which will be produced on the Enterprise edge connector with the specified loadings, and the loads required to be driven by the external device. These loads and timings will not be the same for a device which is attached to the expansion motherboard. Any device which will be required to be used in both system configurations must meet both sets of load and timing details.

This specification is also to be used for testing of the Enterprise 64 and 128 computers. For this purpose the following circuit is to be used as a test load:-



All diodes 1N4148

LS loads	Rl	Cl
1	10k	6pF
2	4k7	12pF
3	3k3	18pF
4	2k4	24pF

Cl includes probe capacitance.

All output logic signals give a maximum low level of 0.4 volts and a minumum high level of 2.4 volts into the specified maximum load. All input logic signals require the same levels to be provided by external circuitry.

Signals prefixed '/' are active low. All other signals are active high.

The loadings specified are the maximum allowable to meet data sheet timings. In some cases this is not the maximum dc load of the driving device, but is limited by the ability of the device to meet ac requirements internal to the computer. Exceeding these loads could cause fatal delays to internal signals.

On power up the operating system examines memory on 16K boundaries to see if RAM is present. Any RAM fitted externally must be decoded down to the 16K level. If it is allowed to echo across any further address space it will be seen by the operating system as being larger than it really is. External ROM's must start on a 256K boundary to be detected by the operating system, but echoing across the unused portion of this 256K space is allowed. I/O space below 80 hex may be used by expansion modules.

External view looking on edge of expansion connector.

SIGNAL	PIN	DESCRIPTION
D0	a14	Active high bi-directional data bus. Used for data exchanges with external memory or I/O devices. Each line can drive 1 LS load with a maximum capacitance of 10pF. External devices driving the bus must be capable of meeting timing and logic level requirements while driving 4 LS inputs and a capacitive load of 45pF. Timing as Z80A data bus.
D1	b14	
D2	a15	
D3	b15	
D4	a16	
D5	b16	
D6	a17	
D7	b17	
A0	a10	Active high address bus. Provides the address within a 16k memory segment or A0-A7 provide the address for one of 256 I/O ports. Each line can drive 2 LS loads with a maximum capacitance of 20pF. Timing as Z80A address bus.
A1	b10	
A2	a11	
A3	b11	
A4	a12	
A5	b12	
A6	a13	
A7	b13	
A8	a6	
A9	b6	
A10	a7	
A11	b7	
A12	a8	
A13	b8	
A14	a9	Active high address bus. Provides the memory segment address. Each line can drive 2 LS loads with a maximum capacitance of 20pF. These signals are delayed by up to 80ns from the Z80A address bus timing, so they may not be stable as /MREQ goes low.
A15	b9	
A16	b26	
A17	a27	
A18	b27	
A19	a28	
A20	b28	
A21	a29	
/RD	a3	Active low read strobe. Used to gate output buffers of memory or I/O devices onto the data bus. Can drive 1 LS load with a maximum capacitance of 10pF. Timing as Z80A /RD.
/WR	b2	Active low write strobe. Used to strobe valid data on the bus into external memory or I/O. Can drive 3 LS loads with a maximum capacitance of 20pF. Timing as Z80A /WR.
/MREQ	a5	Active low memory request. Indicates that the address bus holds a valid address for a memory read or write operation. Can drive 3 LS loads with a maximum capacitance of 20pF. Timing as Z80A /MREQ.

SIGNAL	PIN	DESCRIPTION
/IORQ	b3	Active low input/output request. Indicates that A0-A7 hold a valid address for an input or output operation. Can drive 4 LS loads with a maximum capacitance of 30pF. Timing as Z80A /IORQ.
/RFSH	a2	Active low refresh signal. Indicates that A0-A6 of the address bus hold a 7-bit refresh address and that the current /MREQ may be used to do a refresh cycle to all external dynamic memories. Can drive 4 LS loads with a maximum capacitance of 35pF. Timing as Z80A /RFSH.
/M1	a20	Active low signal indicates that the current machine cycle is the op-code fetch of an instruction execution. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle. Can drive 4 LS loads with a maximum capacitance of 30pF. Timing as Z80A /M1.
/RESET	a18	Active low output. Gives 1ms pulse synchronised to the falling edge of /M1 when reset button pressed or when power first applied to computer. Can drive 2 LS loads with a maximum capacitance of 15pF.
/INT	b18	Active low interrupt input. Must be driven with an open-collector device capable of sinking 2.5mA.
/NMI	b5	Active low non-maskable interrupt input. Must be driven with an open-collector device capable of sinking 2.5mA.
/WAIT	a19	Active low signal indicates that an external device is not ready for a data transfer. Must be driven with an open-collector device capable of sinking 2.5mA. Timing as Z80A /WAIT.
PHI	a22	Z80A clock signal. Nominally 4MHz, with breaks of up to 1.2us when Z80A accesses Nick chip. This signal should only be used for synchronising external events to the CPU, not as a 4MHz clock. Can drive 1 LS load with a maximum capacitance of 10pF.
1MHz	a21	1MHz 50% duty cycle clock output. Can drive 3 LS loads with a maximum capacitance of 30pf.

SIGNAL	PIN	DESCRIPTION
8MHz	a23	8MHz clock output. Can drive 4 LS loads with a maximum capacitance of 30pF.
14MHz	b29	Video dot clock. Varies between 14MHz and 14.25MHz depending on TV colour modulation system. This signal contains frequency jitter at half horizontal line frequency. Can drive 1 ALS load with a maximum capacitance of 8pF.
/HSYNC	a32	Active low horizontal picture sync output. Can drive 10 LS loads.
/VSYNC	b30	Active low vertical picture sync output. Can drive 10 LS loads.
EC0 EC1 EC2 EC3	a24 b24 a25 b25	External colour inputs to Nick palette. Driving device must be capable of sinking 8mA. Only one expansion card may drive these inputs.
/EXTC	a26	Active low external colour enable signal. When active, inputs EC0-3 are output to video display through colour palette of Nick chip. See Nick programming description for details of priority. Driving device must be capable of sinking 8mA. Only one expansion card may drive this input.
L.H.AUDIO	b1	Left-hand channel audio input. 3V pk-pk. into 1k5 for full output.
R.H.AUDIO	a1	Right-hand channel audio input. 3V pk-pk. into 1k5 for full output.
/EXP	b31	Active low expansion data buffer enable. Not connected on computer. This line must be pulled low by an open-collector device in any addressed expansion card to enable data buffers on motherboard. Driving device must be capable of sinking 6mA.
GND	a30,a31 b19,b20 b21,b22 b23,b32	Supply return and logic ground (8 pins).
+5V	a4,b4	These pins are not connected on computer but are used for +5 volt supply on the motherboard.

SIGNAL	PIN	DESCRIPTION
+9V	a33,b33	9 volt DC supply (2 pins). These pins are provided to supply a RAM or disk controller module connected directly to the Enterprise. When a motherboard is connected, it is only used to power the 'computer on' LED.

Bus Timing.
Refer to drg A3PER-1.

SIGNAL	REF	PARAMETER	MIN	MAX
PHI	1	Clock period.	250ns	1500ns
	2	Clock high pulse width.	110ns	1380ns
	3	Clock low pulse width.	110ns	1380ns
A0-A13	4	Low address output delay.		110ns
	5	Low address stable prior to /MREQ (memory cycle).	60ns	
	6	Low address stable prior to /IORQ, /RD or /WR (I/O cycle).	180ns	
	7	Low address stable from /RD,/WR, /IORQ or /MREQ.	75ns	
A14-A21	8	Delay from low address stable to high address stable.		80ns
D0-D7	9	Data output delay.		150ns
	10	Delay to float during write cycle.		90ns
	11	Data setup time, M1 cycle.	35ns	
	12	Data setup time, M2-M5 cycle.	50ns	
	13	Data stable prior to /WR (memory cycle)	80ns	
	14	Data stable prior to /WR (I/O cycle).	-15ns	
	15	Data stable from /WR.	55ns	
	16	Input hold time.	0ns	
/MREQ	17	/MREQ delay from falling edge of clock, /MREQ low.		85ns
	18	/MREQ delay from rising edge of clock, /MREQ high.		85ns
	19	/MREQ delay from falling edge of clock, /MREQ high.		85ns
	20	Pulse width, /MREQ low.	220ns	
	21	Pulse width, /MREQ high.	105ns	
/IORQ	22	/IORQ delay from rising edge of clock, /IORQ low.		75ns
	23	/IORQ delay from falling edge of clock, /IORQ low.		85ns
	24	/IORQ delay from rising edge of clock, /IORQ high.		85ns
	25	/IORQ delay from falling edge of clock, /IORQ high.		85ns

SIGNAL	REF	PARAMETER	MIN	MAX
/RD	26	/RD delay from rising edge of clock, /RD low.		85ns
	27	/RD delay from falling edge of clock. /RD low.		95ns
	28	/RD delay from rising edge of clock, /RD high.		85ns
	29	/RD delay from falling edge of clock, /RD high.		85ns
/WR	30	/WR delay from rising edge of clock, /WR low.		65ns
	31	/WR delay from falling edge of clock, /WR low.		80ns
	32	/WR delay from falling edge of clock, /WR high.		80ns
	33	Pulse width, /WR low.	220ns	
/M1	34	/M1 delay from rising edge of clock, /M1 low.		100ns
	35	/M1 delay from rising edge of clock, /M1 high.		100ns
/RFSH	36	/RFSH delay from rising edge of clock, /RFSH low.		130ns
	37	/RFSH delay from rising edge of clock, /RFSH high.		120ns
/WAIT	38	/WAIT setup time to falling edge of clock.	70ns	
	39	/WAIT hold time from falling edge of clock.	0ns	
/INT	40	/INT setup time to rising edge of clock.	80ns	
	41	/INT hold time from rising edge of clock.	0ns	
/NMI	42	Pulse width, /NMI low.	80ns	
	43	/M1 stable prior to /IORQ (interrupt acknowledge).	560ns	

The above timings assume maximum load on the expansion bus, cartridge with 2 ROM's fitted, and internal 64K RAM expansion board (128K version).

Note that the Dave chip inserts one wait state into each M1 cycle but this may be disabled by software. The Z80A also inserts wait states into I/O accesses and interrupt acknowledge cycles.