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Document .... PER-24
Title ....... Enterprise Peripherals Test Report
Issue ....... 1
Date ........ 11th August 1985
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The tests outlined below were performed specifically on the
following equipment:

Enterprise 128, model 400, serial number LS210
Motherboard issue B, No. 1
RAM card issue B, No. 1
Disk controller issue B, No. 4

Note that the other issue B boards were tried and proven to work.
Issue A boards have also been shown to work (with modifications
incorporated as in issue B). The only problems experienced were
with Enterprises without the additional ground link.


The tests may be grouped into three types:

1) Logical function (ie. that the boards logically conform to the
specification).

2) Timing (ie. that the boards meet the timing requirements of
the Enterprise, as specified in the appropriate document).

3) Noise and other problems not included in (1) and (2) above.


Summary of test stages 1 - 3:

1)   The logical functioning of the three boards has been
established through use in developing the disk software and
frequent general usage of disk and network systems at I.S.

Those signals supplied by the motherboard but not used by current
peripherals were checked. The RAM on the RAM card was tested by
running the modified hot soak test. Additionally, a small program
(listed below) was executed from segment 30H (a RAM card in a
motherboard) to prove M1 cycles without wait states functioned
correctly, since this is the most time-critical cycle.

```
        DI                  ;Disable interrupts
        LD A,8
        OUT (0BFH),A        ;Turn off RAM M1 waits
LOOP    INC A
        OUT (81H),A         ;Flash border continuously
        JR LOOP
```

The ROM socket on the RAM card was tested by running BASIC from
it. The disk controller has been checked extensively during disk
software development/testing.

Additionally, all the pen-plots were checked against circuit
diagrams. Finally, it was proven that it was possible to use six
RAM cards, or five RAM cards plus a disk controller, in a
motherboard and that this configuration worked as expected.

2)    The timing was checked on the early prototypes, and provided that all components are within specification, worst-case calculated timings will be met, with one exception: with a RAM card running in a motherboard, the data setup (REF. 11, document PER-6) on a RAM read cycle is 1ns too short without waits in theory, but easily meets the requirement in practice (see document PER-17). See also test result in section (1) above.

3)    Noise was checked on the motherboard by inserting cards in various slots and measuring ground noise and ringing on the bus (eg. /MREQ, /RD, data and address busses), which were found to be within tolerable levels (ie. below VIL max. when signal is required to be valid). Test results are listed on the following pages.

Power was connected and disconnected to the computer and motherboard numerous times with a disk in a connected drive without causing any corruption of disk data. This problem appears to be solved (although users should be warned not to try this!).

No other problems showed up during testing or in normal use.

Motherboard noise/ringing measurement test results.
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Measurements were made using a 50MHz Hitachi V-509 oscilloscope.
Ground (b20), /RD (a3), /WR (b2), /MREQ (a5), A0 (a10), A8 (a6),
D0 (a14) and D7 (b17) were monitored at two points on the bus (at
slot 1 and slot 6). The highest positive and negative noise peaks
on the ground rail, and the highest positive and negative ringing
peaks after a high-to-low transition on signals were recorded.
Ringing was at a frequency of approximately 40-60MHz. Other
signals were checked at random and found to be similar. All
voltages are relative to ground, pin b20, on the computer
expansion port. Noise pickup on the 'scope probe connected to
it's own ground was about 400mV pk-pk. The measurements were
performed under four load conditions, outlined below, while
running the modified hot soak. A lab PSU provided the 5V supply.

  i) Disk controller in slot 1 (testing segment FC).
 ii) RAM card in slot 1 (testing segment 30).
iii) RAM card in slot 6 (testing segment D0).
 iv) RAM cards in slots 1 to 6 (testing segment 90).

| Signal | Measuring point | Load (i) +ve pk | -ve pk (mV) | Load (ii) +ve pk | -ve pk (mV) |
|--------|-----------------|-----------------|-------------|------------------|-------------|
| Ground | Slot 1 | 350 | -400 | 350 | -400 |
|        | Slot 6 | 450 | -500 | 350 | -400 |
| /RD    | Slot 1 | 750 | -400 | 700 | -400 |
|        | Slot 6 | 750 | -450 | 700 | -500 |
| /WR    | Slot 1 | 700 | -200 | 600 | -100 |
|        | Slot 6 | 700 | -300 | 650 | -200 |
| /MREQ  | Slot 1 | 700 | -100 | 650 | -100 |
|        | Slot 6 | 750 | -250 | 700 | -300 |
| A0     | Slot 1 | 700 | -500 | 650 | -300 |
|        | Slot 6 | 700 | -400 | 800 | -450 |
| A8     | Slot 1 | 700 | -200 | 750 | -350 |
|        | Slot 6 | 750 | -400 | 750 | -450 |
| D0     | Slot 1 | n/a | n/a | 700 | -300 |
|        | Slot 6 | n/a | n/a | 700 | -200 |
| D7     | Slot 1 | n/a | n/a | 650 | -100 |
|        | Slot 6 | n/a | n/a | 700 | -150 |

| Signal | Measuring point | Load (iii) +ve pk | -ve pk (mV) | Load (iv) +ve pk | -ve pk (mV) |
|--------|-----------------|-------------------|-------------|------------------|-------------|
| Ground | Slot 1 | 300 | -350 | 300 | -400 |
|        | Slot 6 | 300 | -400 | 250 | -400 |
| /RD    | Slot 1 | 700 | -450 | 750 | -600 |
|        | Slot 6 | 750 | -650 | 800 | -900 |
| /WR    | Slot 1 | 700 | -250 | 700 | -500 |
|        | Slot 6 | 700 | -500 | 750 | -750 |
| /MREQ  | Slot 1 | 650 | -450 | 650 | -400 |
|        | Slot 6 | 750 | -500 | 700 | -750 |
| A0     | Slot 1 | 700 | -400 | 800 | -550 |
|        | Slot 6 | 650 | -450 | 800 | -750 |
| A8     | Slot 1 | 650 | -300 | 750 | -400 |
|        | SLot 6 | 750 | -500 | 800 | -600 |
| D0     | Slot 1 | 550 | -100 | 650 | -450 |
|        | Slot 6 | 600 | -200 | 700 | -450 |
| D7     | Slot 1 | 550 | -200 | 700 | -300 |
|        | Slot 6 | 600 | -100 | 700 | -300 |