CONFIDENTIAL - INTELLIGENT SOFTWARE & ENTERPRISE COMPUTERS LTD.

Document PER-18
Title ..... Enterprise 64/128 Disk Controller Module
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The Enterprise 64/128 disk controller module interfaces up to four 5-1/4" or 3-1/2" (300 rpm) disk drives to the Enterprise 64/128 expansion bus.

The module is designed around the Western Digital WD1770 floppy disk controller/formatter chip, and also holds a 16K x 8 ROM (optionally 32K x 8) which contains the disk software. For programming information refer to the WD1770 data sheet.

The module is designed to connect either directly to the computer via the interface cable, or else to plug into any slot on the motherboard.

Connection to the disk drives is by a 34 way ribbon cable with IDC socket, which mates with a PCB mounted plug on the module. Drives are connected in parallel on this cable with the drive furthest from the controller having pull-up resistors on all the controller output lines.

The disk controller module must not be connected or disconnected from the computer or motherboard with power applied to the system. The motherboard must be powered before the computer in order that the operating system may log in the disk controller module.

M1 wait states are automatically inserted by the operating system, and these are required by the 250ns ROM.

The ROM maps into the bottom of the 512K memory space allocated to the module. The printed wiring board is tracked to take a 16K x 8 ROM, but expansion to 32K x 8 is provided for by simple linking on the board. The ROM echoes across the lower 256K but is inhibited from the higher part of the memory space. The controller registers and I/O buffers map into the 16 I/O bytes allocated to the module, with the controller echoing across the lower 8 bytes and the I/O ports echoing across the higher 8 bytes.

A module attached directly to the computer maps as if it were in slot 1 of a motherboard.

SLOT	ROM	CONTROLLER	I/O
1	080000H-083FFFH	10H-13H	18H
2	100000H-103FFFH	20H-23H	28H
3	180000H-183FFFH	30H-33H	38H
4	200000H-203FFFH	40H-43H	48H
5	280000H-283FFFH	50H-53H	58H
6	300000H-303FFFH	60H-63H	68H

Circuit operation:

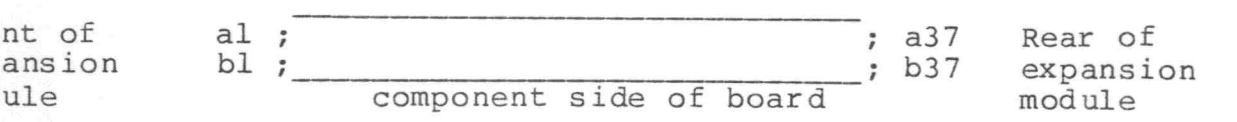
U5, U6, U7, U8, and U9 decode the ROM and I/O spaces and generate chip- and output-enables. U3 buffers the data bus for ROM (U2), disk controller (U1) and port (U4, U10) reads and writes. U11, U12 and U13 drive the disk drive bus outputs. R4-9 are pull-ups (terminators) for disk drive bus inputs.

For details of the WD1770 registers refer to the Western Digital data sheet. The input and output ports (same address) are connected as follows:-

Output.	b7	In use.
	b6	Disk change reset.
	b5	0 = double density, 1 = single density.
	b4	Side 1 select.
	b3	Select drive 3.
	b2	Select drive 2.
	b1	Select drive 1.
	b0	Select drive 0.
Input.	b7	Data request from WD1770.
	b6	Disk change.
	b5	Not used.
	b4	Not used.
	b3	Not used.
	b2	Not used.
	b1	Interrupt request from WD1770.
	b0	Drive ready.

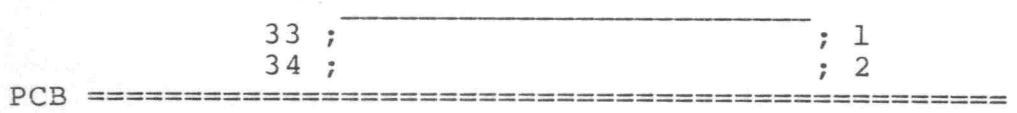
Signals prefixed '/' are active low. All other signals are active high. All connector pins which are not mentioned are not connected.

View looking on edge of disk controller module connector fingers.



Note that pins a34,b34 are reserved for possible use as a polarizing position.

View looking on pins of disk drive connector.



COMPUTER INTERFACE

SIGNAL	PIN	DESCRIPTION
D0	a14	Active high bi-directional data bus. Module is 1 LS load, and is capable of driving 11 LS loads.
D1	b14	
D2	a15	
D3	b15	
D4	a16	
D5	b16	
D6	a17	
D7	b17	
A0	a10	Active high address bus. Module load is different for various address lines, with a worst case of 2 LS inputs plus 6pF capacitive load.
A1	b10	
A2	a11	
A3	b11	
A4	a12	
A5	b12	
A6	a13	
A7	b13	
A8	a6	
A9	b6	
A10	a7	
A11	b7	
A12	a8	
A13	b8	
A14	a9	
A18	b27	
A19	a28	
A20	b28	
A21	a29	
/RD	a3	Active low read strobe. Module is 1 LS load.
/WR	b2	Active low write strobe. Module is 2 LS loads plus 6pF capacitive load.
/MREQ	a5	Active low memory request. Indicates that the address bus holds a valid address for a memory read operation. Module is 1 LS load.
/IORQ	b3	Active low input/output request. Indicates that A0-A7 hold a valid address for an input or output operation. Module is 1 LS load.

SIGNAL	PIN	DESCRIPTION
/EXP	b31	Active low expansion data buffer enable. This line is pulled low by an open-collector driver in the disk controller module which is capable of sinking 8mA.
/RESET	a18	Active low input resets WD1770 and clears output port to deselect all disk drives. Module is 1 LS load plus 6pF capacitive load.
8MHz	a23	Continuous 8MHz clock input. Module is 10pF capacitive load only.
SA0 SA1 SA2	b35 a36 b36	Static slot address inputs, to be externally wired high or low with binary slot number. These lines are compared with A19-A21 for memory access and A4-A6 for I/O access to enable the module.
GND	b19,b20 b21,b22 b23,a30 a31,b32 a33,b33 a35	Supply return and logic ground (11 pins).
+5V	a4,b4	5 volt supply.
N/C	a34,b34	May be used as a polarizing position.

ALL OTHER EDGE CONNECTOR PINS ARE NOT CONNECTED

DISK DRIVE INTERFACE

All the following outputs are open collector capable of sinking 40mA. All inputs are either 1 LS load or capacitive load only pulled to +5 volts with a 470R resistor. All signals are active low.

PIN	I/O	DESCRIPTION
1	O	Disk change reset. Active signal resets disk changed latch present in some drives. This signal may be grounded by drives which do not use it. (*)
2	I	Disk changed. Output from latch present in some drives, otherwise open-circuit. (*)

PIN	I/O	DESCRIPTION
4	O	In use. Supported in hardware but not used by the software, as the drive can be set up not to require it. (*)
6	O	Select drive 3. True for drive 3 selected.
8	I	Index pulse. See WD1770 specification.
10	O	Select drive 0. True for drive 0 selected.
12	O	Select drive 1. True for drive 1 selected.
14	O	Select drive 2. True for drive 2 selected.
16	O	Motor on. See WD1770 specification.
18	O	Step direction. See WD1770 specification.
20	O	Step pulse. See WD1770 specification.
22	O	Write data. See WD1770 specification.
24	O	Write gate. See WD1770 specification.
26	I	Track 0. See WD1770 specification.
28	I	Write protect. See WD1770 specification.
30	I	Read data. See WD1770 specification.
32	O	Select side 1. True for side one selected.
34	I	Ready. Not all drives provide this signal. (*)
3,5 7,9 11,13 15,17 19,21 23,25 27,29 31,33		Ground and signal return.

Pins marked with a (*) are optional and need not be supported. (See later section for a fuller explanation).

The following parameters are to be used for the testing of the disk controller module.

COMPUTER INTERFACE

Required Bus Timing.
Refer to drg A3PER-5.
(Timings apply with the use of specified components operating at a maximum temperature of 70 degrees Celsius.)

REF	PARAMETER	MIN	MAX
1	Low address stable to data out. (ROM read)		262ns
2	High address stable to data out. (ROM read)		307ns
3	/MREQ low to stable data out. (ROM read)		292ns
4	/RD low to stable data out. (ROM read)		134ns
5	High address stable to /EXP low. (ROM read)		105ns
6	/MREQ low to /EXP low. (ROM read)		90ns
7	Data hold from /MREQ. (ROM read)	13.5ns	
8	Data hold from /RD. (ROM read)	11ns	
9	/MREQ high to data float. (ROM read)		85ns
10	/RD high to data float. (ROM read)		47ns
11	/MREQ high to /EXP high. (ROM read)		90ns
12	Low address stable to data out. (Input)		262ns
13	/IORQ low to stable data out. (Input)		264ns
14	/RD low to stable data out. (Input)		286ns
15	/IORQ low to /EXP low. (Input/output)		90ns
16	/RD low to /EXP low. (Input)		112ns
17	Data hold from /IORQ. (Input)	26ns	
18	Data hold from /RD. (Input)	11ns	
19	/IORQ high to data float. (Input)		85ns
20	/RD high to data float. (Input)		47ns
21	/IORQ high to /EXP high. (Input/output)		90ns
22	/RD high to /EXP high. (Input)		112ns
23	Low address stable to /EXP low. (Input/output)		105ns
24	Low address stable prior to /WR low. (Output)	50ns	
25	/WR low to /EXP low. (Output)		90ns
26	Data stable prior to /WR high. (Output)	162ns	
27	Data hold from /WR high. (Output)	23ns	
28	Low address hold from /WR high. (Output)	27ns	
29	/WR high to /EXP high. (Output)		90ns

Maximum supply current 550mA at 5.25V.

DISK DRIVE INTERFACE

The timing of disk interface signals is dependent on the WD1770 and controlling software.

The following are timing limitations on a drive must be met for DISKIO and the WD1770 to read and write to it.

1) The motor must be at 300rpm (+/- 3%) within 1 second of a drive-select being issued.

2) The drive must be able to accept step commands within 30ms of being selected.

3) The head must load in less than 50 ms after a drive-select and/or motor-on command.

4) The data rates supported are 125 Kbits/sec (FM) and 250 Kbits/sec (MFM) (see the WD1770 specification).

5) The maximum time to reach the outermost track must be less than 1.3 seconds.

6) The drive must be triggered by a change in level (not edge-triggered).

7) After a ready signal it is assumed that the drive can successfully execute a read or a write instruction after 50ms.

8) The drive must be able to step faster than 30ms per step (a limitation of the WD1770).

9) The drive must be accept/provide all the signals mentioned in the section Disk Drive Interface above (note that some are optional - see Optional Connections below).

The disk controller has worked successfully with the following drives:

3-1/2 inch: Epson SMD100
Epson SMD120
Epson SMD130
Epson SMD140
Sony MPX-026R
BASF 6162
Teac FD35B
Teac FD35F

5-1/4 inch: Shugart SA465
BASF 6128
Mitsubishi M4853

Optional Connections

The performance of the disk driving software is improved by the presence of these connections, however it can function correctly without them being used.

The 'disk change' and 'disk change reset' lines are read and acted upon but if the disk change line remains false then DISKIO will function but without being able to sense a change of disk. Note that if disk drives with and without disk-change detect are mixed, the software will not be able to utilise this facility.

The 'in use' line is not used; it is assumed that the drive has been, or can be set up so an indicator of activity (ie. an LED) is activated by a drive-select and/or motor-on.

The software looks for a transition on the 'ready' line. If ready is activated by a drive-select then this will impair the function of the system but not prevent it. The software assumes that 50 ms after ready becomes true the disk can be accesssed for reading or verifying.