CONFIDENTIAL - INTELLIGENT SOFTWARE & ENTERPRISE COMPUTERS LTD.

Document PER-17
Title ..... Enterprise 64/128 64K RAM Expansion Module
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The Enterprise 64/128 64K RAM expansion module contains 64K x 8 of dynamic RAM and a socket which is strappable to take a user EPROM of up to 32K x 8. The module is designed to connect either directly to the computer via the interface cable, or else to plug into any slot on the motherboard.

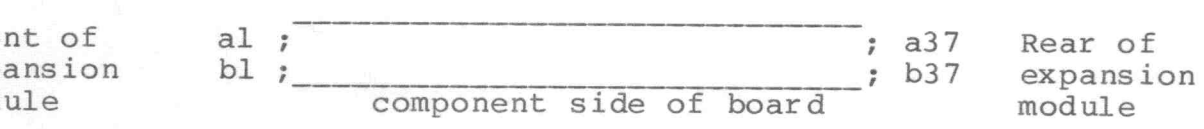
M1 wait states are normally inserted by the operating system, and these are required by the 250ns EPROM. However, the speed of the RAM allows it to be used with no wait states. (In theory, a RAM M1 read cycle without waits fails to meet the required data setup time on the Z80 by 1ns. However, this figure is obtained by taking the worst case timings into full load for each device in the signal path. Since there are several devices in the path, none of which are fully loaded, there is no problem in practice.)

EPROMS which can be accepted are 2764, 27128 or 27256, meeting the Intel specification for a 250ns part.

The 512K space allocated to the module is divided into two halves with the EPROM occupying the bottom 64K of the lower half, and the RAM occupying the bottom 64K of the top half. EPROM's echo all across this 64K memory space. A module attached directly to the computer maps as if it were in slot 1 of a motherboard.

SLOT	EPROM	RAM
1	080000H-08FFFFH	0C0000H-0CFFFFH
2	100000H-10FFFFH	140000H-14FFFFH
3	180000H-18FFFFH	1C0000H-1CFFFFH
4	200000H-20FFFFH	240000H-24FFFFH
5	280000H-28FFFFH	2C0000H-2CFFFFH
6	300000H-30FFFFH	340000H-34FFFFH

View looking on edge of RAM module connector fingers.



Note that pins a34,b34 are reserved for use as a possible polarizing position.

Circuit operation:

U13 and U14 decode the RAM and ROM address spaces. U15 and U16 generate /RAS and /CAS for the DRAM from the /MREQ signal, select row/column addresses and provide ROM/buffer enables. U11 and U12 multiplex the address bus and U10 buffers the data bus for ROM (U9) and RAM (U1-8) reads. Resistor pack RP1 pulls the buffer inputs high when the ROM and RAM are deselected to prevent noise or oscillation as the buffer is turned on. R4 slows the rise-time of /RAS and limits ringing.

The 64K RAM expansion module must not be connected or disconnected from the computer or motherboard with power applied to the system. The motherboard or expansion power supply must be powered before the computer in order that the operating system may log in the RAM expansion module.

Signals prefixed '/' are active low. All other signals are active high. All edge connector pins which are not mentioned are not connected.

SIGNAL	PIN	DESCRIPTION
D0	a14	Active high bi-directional data bus. Module is a 10pF capacitive load only, and is capable of driving 11 LS loads.
D1	b14	
D2	a15	
D3	b15	
D4	a16	
D5	b16	
D6	a17	
D7	b17	
A0	a10	Active high address bus. Module load is different for various address lines, with a worst case of 1 LS input plus 6pF capacitive load.
A1	b10	
A2	a11	
A3	b11	
A4	a12	
A5	b12	
A6	a13	
A7	b13	
A8	a6	
A9	b6	
A10	a7	
A11	b7	
A12	a8	
A13	b8	
A14	a9	
A15	b9	
A16	b26	
A17	a27	
A18	b27	
A19	a28	
A20	b28	
A21	a29	
/RD	a3	Active low read strobe. Module is 1 LS load plus 7pF capacitive load.
/WR	b2	Active low write strobe. Module is 1 LS load.
/MREQ	a5	Active low memory request. Indicates that the address bus holds a valid address for a memory read or write operation. Module is 2 LS loads.
/EXP	b31	Active low expansion data buffer enable. This line is pulled low by an open-collector driver in the RAM expansion module which is capable of sinking 8mA.

SIGNAL	PIN	DESCRIPTION
SA0 SA1 SA2	b35 a36 b36	Static slot address inputs, to be externally wired high or low with binary slot number. These inputs are compared with A19-A21 to enable the module.
GND	b19,b20 b21,b22 b23,a30 a31,b32 a33,b33 a35	Supply return and logic ground (11 pins).
+5V	a4,b4	5 volt supply.
N/C	a34,b34	May be used for a polarizing slot.

ALL OTHER PINS ARE NOT CONNECTED

The following parameters are to be used for the testing of the 64k RAM expansion module.

Required Bus Timing.
Refer to drg A3PER-4.
(Timings apply with the use of specified components operating at a maximum temperature of 70 degrees Celsius.)

REF	PARAMETER	MIN	MAX
1	Address stable to data out stable. (EPROM read)		336ns
2	/MREQ low to data out stable. (EPROM read)		300ns
3	/RD low to data out stable. (EPROM read)		118ns
4	High address stable to /EXP low.		118ns
5	/MREQ low to /EXP low.		82ns
6	Data hold from /MREQ.	12ns	
7	Data hold from /RD.	6ns	
8	Data float from /MREQ.		80ns
9	Data float from /RD.		47ns
10	/MREQ high to /EXP high.		63ns
11	/MREQ high period.	100ns	
12	A0-A7 stable prior to /MREQ. (RAM cycle)	5ns	
13	A8-A21 stable prior to /MREQ. (RAM cycle)	-36ns	
14	/MREQ low to data out stable. (RAM read)		234ns
15	/RD low to data out stable. (RAM read)		42ns
16	/WR low period. (RAM write)	50ns	
17	Data setup to /WR low. (RAM write)	-5ns	
18	/MREQ low prior to data stable. (RAM write)		36ns
19	Data hold from /MREQ low. (RAM write)	161ns	
20	Data hold from /WR low. (RAM write)	65ns	

Maximum supply current: 325mA at 5.25V (no ROM fitted).