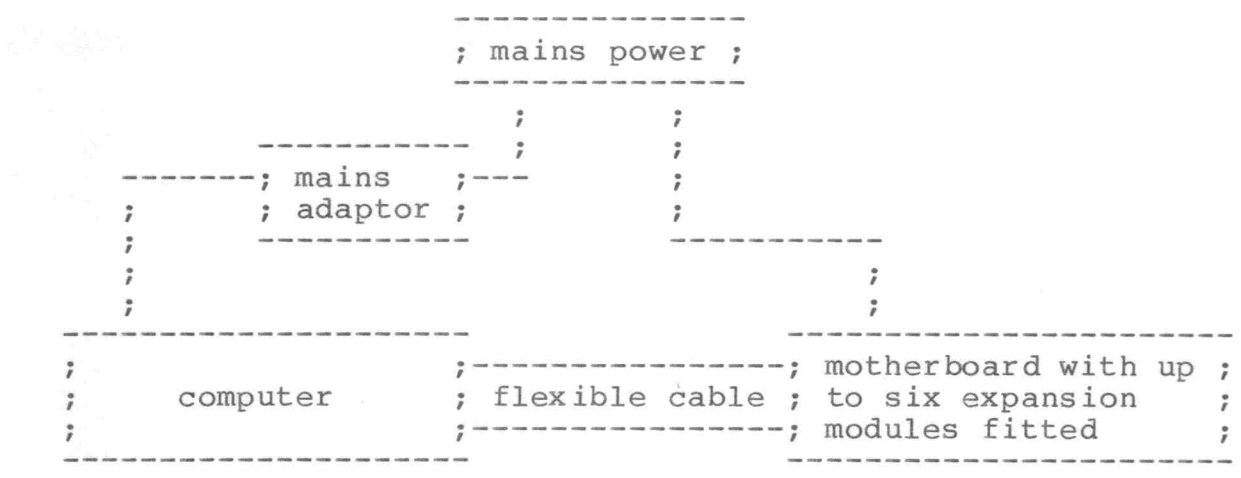
Document PER-12
Title ..... ENTERPRISE 64/128 SYSTEM EXPANSION
PROVISIONAL SPECIFICATION
Issue 1
Date 11-APR-85

Contents

System Expansion with Motherboard

A six-slot motherboard is connected to the computer expansion bus via a flexible ribbon cable with a pcb edge connector at each end. Expansion modules plug into and draw power from the motherboard, which has its own internal supply generating +5 volts, +12 volts, and -12 volts.

The motherboard is complete with power cable, power fuse and on/off switch. The computer must still be powered from its original mains adaptor. Modules to be plugged into the motherboard must meet the timing and maximum load specifications given in document PER-7.

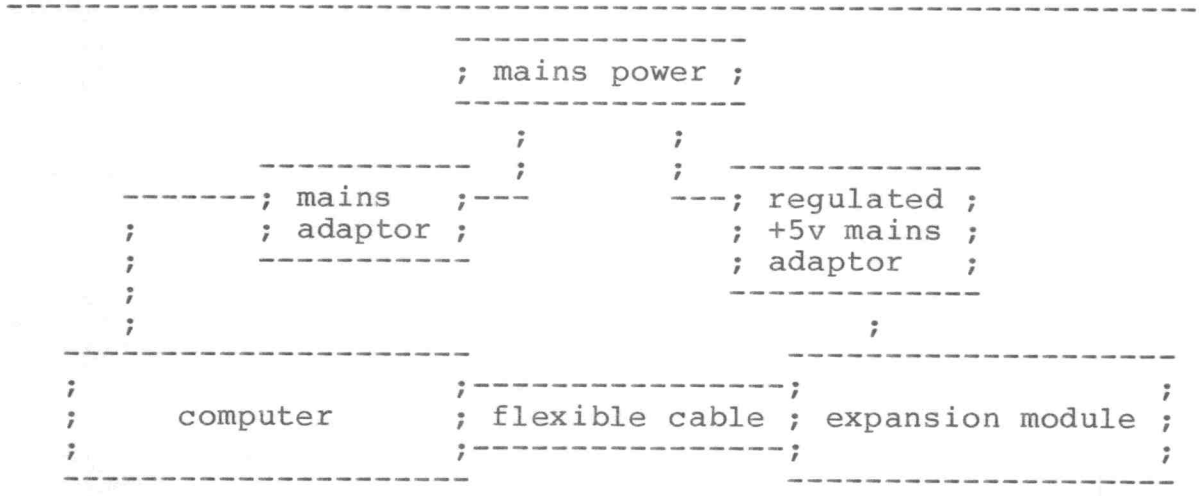


SYSTEM EXPANSION WITH MOTHERBOARD

System Expansion without Motherboard

A single expansion module is connected to the computer by means of the same flexible cable as used for connecting the computer to the motherboard. Power is supplied to the module from an external regulated +5 volt 500mA mains adaptor which connects to the expansion module through a power jack. This jack is of a different design to the one on the computer to prevent incorrect connection, and is arranged so that if a module is powered from the regulated adaptor while being fitted in the motherboard then the +5 volt supply from the motherboard will be disconnected to prevent supply conflict.

An expansion module connected in this way will appear in the same memory and IO space as if it were inserted in slot 1 of a motherboard. The + and - 12 volt supplies are not available for a module in this system configuration. The module should meet the timing and maximum load specifications given in document PER-6.



SYSTEM EXPANSION WITHOUT MOTHERBOARD

It is important for either expansion system that power is applied to the expansion module or motherboard before the computer, as the operating system only looks for peripheral devices on a cold reset. If power is applied simultaneously, or to the computer first, the reset button will need to be pressed twice to log in the expansion modules.

If an expansion module is connected directly to the computer and the full available bus driving ability is used by the module then power should not be applied for any length of time to the expansion module without powering the computer, else there is a slight possibility of damage occuring to MOS devices in the computer. Conversely, if power is left applied to the computer without power on a directly connected expansion module, MOS devices in the expansion module which are not buffered from the bus by TTL chips may suffer damage. This is not a problem if the motherboard is used, as the ALS buffers in the motherboard are able to withstand voltage on their inputs while unpowered, and the 0.2mA maximum input curent of the buffers in the low state is too small to cause damage to the unpowered devices in the computer. The only danger is the motherboard data buffer, but with no power on the computer this will be disabled.

Power Supplies

1. The motherboard PSU will provide power for up to six expansion cards. As a complete ready-assembled unit residing within the motherboard enclosure, it must generate regulated 5V and +/-12V outputs with a total power output of 17W maximum. A switch-mode design is preferred.

The unit should operate from 220V/240V nominal mains, and cope with a 20ms line drop-out. It will ideally incorporate an on/off switch, indicator and fuse. If a switch-mode type is used, the switching frequency should be above 20kHz with adequate EMI screening provided.

The required outputs are 5V @ 2.75A and +/-12V @ 100mA with 5% and 10% tolerance respectively (including line/load regulation and ripple).

2. In order to power an expansion RAM or disk card connected directly to the Enterprise (ie. without a motherboard), a 5V power source will be required. This is to be provided in the form of a separately-housed mains adaptor with a regulated 5V DC output which would plug into the expansion card unit. A different jack would be used to prevent accidental swapping of this and the 9V mains adaptor of the computer. The jack input would also switch out the bus 5V rail to prevent damage being caused by plugging the 5V adaptor into a card installed in the motherboard.

This unit will also run off 220V/240V mains but need only generate 5V @ 500mA with 5% tolerance (as above). It can be a simple linear supply consisting of a transformer, rectifier, capacitor and regulator.

Enterprise 64/128 Motherboard Bus

1. Introduction

This specification is to be used for modules which are required to be attached to the Enterprise expansion motherboard. It details the signals which will be produced on the motherboard edge connectors with the specified loadings, and the loads required to be driven by the expansion modules. These loads and timings will not be the same for a device which is to be attached directly to the Enterprise expansion bus without the use of the motherboard. Any device which will be required to be used in both system configurations must meet both sets of load and timing details.

Buffer ICs used in the motherboard are all ALS types, to keep added signal delays to an absolute minimum, and to keep the load on the computer edge connector as light as possible. All signals from the computer to expansion modules are buffered with the exception of the picture synchronisation pulses, which are not edge critical and can already drive 10 LS loads. With the exception of the data bus, signals into the computer are not buffered.

The following load specifications are the maximum that may be presented by any single expansion module so as not to overload the motherboard bus with six modules fitted. The specification for the data bus is not the maximum that can be driven by the ALS buffers in the motherboard, but is specified so that an LS device in an expansion module can drive the load of the motherboard buffers plus five other expansion modules.

All output logic signals give a maximum low level of 0.4 volts and a minumum high level of 2.4 volts into the specified maximum load. All input logic signals require the same levels to be provided by external circuitry.

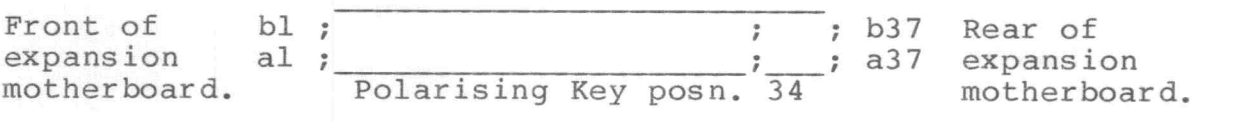
Signals prefixed '/' are active low. All other signals are active high.

2. On power up the operating system examines memory on 16k boundaries to see if ram is present. Any ram fitted externally must be decoded down to the 16k level. If it is allowed to echo across any further address space it will be seen by the operating system as being larger than it really is. External roms must start on a 256k boundary to be detected by the operating system, but echoing across the unused portion of this 256k space is allowed. I/O space below 80 hex may be used by expansion modules. The motherboard allocates 512k bytes of memory space and 16 bytes of IO space to each expansion module by the use of three slot-address pins which are hard-wired high or low according to the slot position. These levels must compare with the highest relevant address lines (memory A19-A21, IO A4-A6) to select the module.

SLOT	MEMORY ADDRESS	IO ADDRESS
1	080000H-0FFFFFH	10H-1FH ← EXDOS ROM
2	100000H-17FFFFH	20H-2FH ←
3	180000H-1FFFFFH	30H-3FH
4	200000H-27FFFFH	40H-4FH
5	280000H-2FFFFFH	50H-5FH
6	300000H-37FFFFH	60H-6FH

Memory addresses 0H-7FFFFH and 380000H-3FFFFFH are reserved for use by the main computer. IO addresses 80H-FFH are also reserved for future enhancements, but IO addresses 0H-FH and 70H-7FH may be used by expansion modules although this is not recomended as different modules using these addresses could cause bus conflict.

View looking down on motherboard expansion module connector.



3. Bus Specification

SIGNAL	PIN	DESCRIPTION
D0	a14	Active high bi-directional data bus. Used for data exchanges with external memory or I/O devices. Each line can drive 2 LS loads per module. Expansion modules driving the bus must be capable of meeting timing and logic level requirements while driving 11 LS inputs.
D1	b14	
D2	a15	
D3	b15	
D4	a16	
D5	b16	
D6	a17	
D7	b17	
A0	a10	Active high address bus. Provides the address within a 16k memory segment or A0-A7 provide the address for one of 256 I/O ports. Each line can drive 4 LS loads per module.
A1	b10	
A2	a11	
A3	b11	
A4	a12	
A5	b12	
A6	a13	
A7	b13	
A8	a6	
A9	b6	
A10	a7	
A11	b7	
A12	a8	
A13	b8	
A14	a9	Active high address bus. Provides the memory segment address. Each line can drive 4 LS loads per module. These lines may not be stable as /MREQ goes low.
A15	b9	
A16	b26	
A17	a27	
A18	b27	
A19	a28	
A20	b28	
A21	a29	
/RD	a3	Active low read strobe. Used to gate output buffers of memory or I/O devices onto the data bus. Can drive 4 LS loads per module.
/WR	b2	Active low write strobe. Used to strobe valid data on the bus into external memory or I/O. Can drive 4 LS loads per module.
/MREQ	a5	Active low memory request. Indicates that the address bus holds a valid address for a memory read or write operation. Can drive 4 LS loads per module.
/IORQ	b3	Active low input/output request. Indicates that A0-A7 hold a valid address for an input or output operation. Can drive 4 LS loads per module.

SIGNAL	PIN	DESCRIPTION
/RFSH	a2	Active low refresh signal. Indicates that A0-A6 of the address bus hold a 7-bit refresh address and that the current /MREQ may be used to do a refresh cycle to all external dynamic memories. Can drive 4 LS loads per module.
/M1	a20	Active low signal indicates that the current machine cycle is the op-code fetch of an instruction execution. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle. Can drive 4 LS loads per module.
/RESET	a18	Active low output. Gives 1mS pulse synchronised to the falling edge of /M1 when reset button pressed or when power first applied to computer. Can drive 4 LS loads per module.
/INT	b18	Active low interrupt input. Must be driven with an open-collector device capable of sinking 2.5mA.
/NMI	b5	Active low non-maskable interrupt input. Must be driven with an open-collector device capable of sinking 2.5mA.
/WAIT	a19	Active low signal indicates that an external device is not ready for a data transfer. Must be driven with an open-collector device capable of sinking 2.5mA.
PHI	a22	Z80A clock signal. Nominally 4MHz, with breaks of up to 1.2uS when Z80A accesses Nick chip. This signal should only be used for synchronising external events to the cpu, not as a 4MHz clock. Can drive 4 LS loads per module.
1MHz	a21	1MHz 50% duty cycle clock output. Can drive 4 LS loads per module.
8MHz	a23	8MHz clock output. Can drive 4 LS loads per module.
14MHz	b29	Video dot clock. Varies between 14MHz and 14.25MHz depending on TV colour modulation system. This signal contains frequency jitter at half horizontal line frequency. Can drive 1 LS load per module.

SIGNAL	PIN	DESCRIPTION
/HSYNC	a32	Active low horizontal picture sync output. Can drive 1 LS load per module.
/VSYNC	b30	Active low vertical picture sync output. Can drive 1 LS load per module.
EC0 EC1 EC2 EC3	a24 b24 a25 b25	External colour inputs to Nick palette. Driving device must be capable of sinking 8mA. Only one expansion card may drive these inputs.
/EXTC	a26	Active low external colour enable signal. When active, inputs EC0-3 are output to video display through colour palette of Nick chip. See Nick programming description for details of priority. Driving device must be capable of sinking 8mA. Only one expansion card may drive this input.
L.H.AUDIO	b1	Left-hand channel audio input. 3V p.t.p. into 1k5 for full output. Only one expansion card may drive this input.
R.H.AUDIO	a1	Right-hand channel audio input. 3V p.t.p. into 1k5 for full output. Only one expansion card may drive this input.
/EXP	b31	Active low expansion data buffer enable. This line must be pulled low by an open-collector device in any addressed expansion module to enable data buffers on motherboard. Driving device must be capable of sinking 6mA.
GND	b19,b20 b21,b22 b23,a30 a31,b32 a33,b33 a35	Supply return and logic ground.(11 pins).
+12V	a37	Positive 12 volt +/- 10% supply provided by motherboard. A maximum of 100mA is available to power all six expansion modules. This supply is not provided for modules which connect directly to the computer.

SIGNAL	PIN	DESCRIPTION
-12V	b37	Negative 12 volt +/- 10% supply provided by motherboard. A maximum of 100mA is available to power all six expansion modules. This supply is not provided for modules which connect directly to the computer.
+5V	a4,b4	Positive 5 volt +/- 5% supply provided by motherboard. A maximum of 2.75 Amps is available to power all six expansion modules. This supply is not provided for modules which connect directly to the computer. An external supply is provided through a power jack on the module case.
SA0 SA1 SA2	b35 a36 b36	Slot address inputs. These pins are hard-wired on the motherboard with the binary slot number (left slot = 1, right slot = 6). These inputs should be compared with A19-A21 during memory accesses and compared with A4-A6 during IO accesses to enable the expansion module. A module connected directly to the computer without the motherboard will have these lines wired as slot 1.

Bus Timing.
Refer to drg A3PER1.

SIGNAL	REF	PARAMETER	MIN	MAX
PHI	1	Clock period.	250nS	1500nS
	2	Clock high pulse width.	110nS	1380nS
	3	Clock low pulse width.	110nS	1380nS
A0-A13	4	Low address output delay.		117nS
	5	Low address stable prior to /MREQ (memory cycle).	53nS	
	6	Low address stable prior to /IORQ, /RD or /WR (IO cycle).	173nS	
	7	Low address stable from /RD,/WR, /IORQ or /MREQ.	68nS	
A14-A21	8	Delay from low address stable to high address stable.		87nS
D0-D7	9	Data output delay.		157nS
	10	Delay to float during write cycle.	Not Applicable	
	11	Data setup time, M1 cycle.	28nS	
	12	Data setup time, M2-M5 cycle.	43nS	
	13	Data stable prior to /WR (memory cycle).	73nS	
	14	Data stable prior to /WR (IO cycle).	-52nS	
	15	Data stable from /WR.	48nS	
	16	Input hold time.	7nS	
/MREQ	17	/MREQ delay from falling edge of clock, /MREQ low.	13nS	92nS
	18	/MREQ delay from rising edge of clock, /MREQ high.		92nS
	19	/MREQ delay from falling edge of clock, /MREQ high.		92nS
	20	Pulse width, /MREQ low.	220nS	
	21	Pulse width, /MREQ high.	105nS	
/IORQ	22	/IORQ delay from rising edge of clock, /IORQ low.		82nS
	23	/IORQ delay from falling edge of clock, /IORQ low.		92nS
	24	/IORQ delay from rising edge of clock, /IORQ high.		92nS
	25	/IORQ delay from falling edge of clock, /IORQ high.		92nS

SIGNAL	REF	PARAMETER	MIN	MAX
/RD	26	/RD delay from rising edge of clock, /RD low.		92nS
	27	/RD delay from falling edge of clock. /RD low.		102nS
	28	/RD delay from rising edge of clock, /RD high.		92nS
	29	/RD delay from falling edge of clock, /RD high.		92nS
/WR	30	/WR delay from rising edge of clock, /WR low.		72nS
	31	/WR delay from falling edge of clock, /WR low.		87nS
	32	/WR delay from falling edge of clock, /WR high.		87nS
	33	Pulse width, /WR low.	220nS	
/M1	34	/M1 delay from rising edge of clock, /M1 low.		107nS
	35	/M1 delay from rising edge of clock, /M1 high.		107nS
/RFSH	36	/RFSH delay from rising edge of clock, /RFSH low.		137nS
	37	/RFSH delay from rising edge of clock, /RFSH high.		127nS
/WAIT	38	/WAIT setup time to falling edge of clock.	80nS	
	39	/WAIT hold time from falling edge of clock.	-3nS	
/INT	40	/INT setup time to rising edge of clock.	90nS	
	41	/INT hold time from rising edge of clock.	-3nS	
/NMI	42	Pulse width, /NMI low.	80nS	
	43	/M1 stable prior to /IORQ (interrupt acknowledge).	553nS	

The above timings assume maximum load on the motherboard, i.e. 6 modules fitted each with maximum input loads.

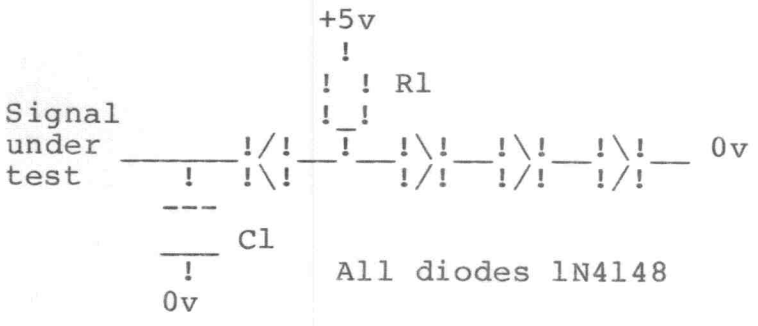
Under standard operating system programming the Dave chip inserts one wait state into each M1 cycle which adds 250ns to the access time of memory on the motherboard bus, but this may be disabled by software. The Z80A also inserts wait states into IO accesses and interrupt acknowledge cycles.

Enterprise 64/128 Expansion Port Definition

1. Introduction

This specification is to be used for modules which are required to be connected directly to the Enterprise expansion bus without use of the expansion motherboard. It defines the signals which will be produced on the Enterprise edge connector with the specified loadings, and the loads required to be driven by the external device. These loads and timings will not be the same for a device which is attached to the expansion motherboard. Any device which will be required to be used in both system configurations must meet both sets of load and timing details. The product shall conform to this specification for successful operation of expansion modules and units.

This specification can be used for testing of the Enterprise 64 and 128 computers. For this purpose the following circuit is to be used as a test load:-



LS loads	Rl	Cl
1	10k	6pF
2	4k7	12pF
3	3k3	18pF
4	2k4	24pF

Cl includes probe capacitance.

Standard Load Test Circuit

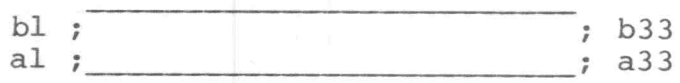
All output logic signals give a maximum low level of 0.4 volts and a minumum high level of 2.4 volts into the specified maximum load. All input logic signals require the same levels to be provided by external circuitry.

Signals prefixed '/' are active low. All other signals are active high.

The loadings specified are the maximum allowable to meet data sheet timings. In some cases this is not the maximum dc load of the driving device, but is limited by the ability of the device to meet ac requirements internal to the computer. Exceeding these loads could cause fatal delays to internal signals.

2. On power up the operating system examines memory on 16k boundaries to see if ram is present. Any ram fitted externally must be decoded down to the 16k level. If it is allowed to echo across any further address space it will be seen by the operating system as being larger than it really is. External roms must start on a 256k boundary to be detected by the operating system, but echoing across the unused portion of this 256k space is allowed. I/O space below 80 hex may be used by expansion modules.

External view looking on edge of expansion connector.



3. Bus Specification

SIGNAL	PIN	DESCRIPTION
D0	a14	Active high bi-directional data bus. Used for data exchanges with external memory or I/O devices. Each line can drive 1 LS load with a maximum capacitance of 10pF. External devices driving the bus must be capable of meeting timing and logic level requirements while driving 4 LS inputs and a capacitive load of 45pF. Timing as Z80A data bus.
D1	b14	
D2	a15	
D3	b15	
D4	a16	
D5	b16	
D6	a17	
D7	b17	
A0	a10	Active high address bus. Provides the address within a 16k memory segment or A0-A7 provide the address for one of 256 I/O ports. Each line can drive 2 LS loads with a maximum capacitance of 20pF. Timing as Z80A address bus.
A1	b10	
A2	a11	
A3	b11	
A4	a12	
A5	b12	
A6	a13	
A7	b13	
A8	a6	
A9	b6	
A10	a7	
A11	b7	
A12	a8	
A13	b8	
A14	a9	Active high address bus. Provides the memory segment address. Each line can drive 2 LS loads with a maximum capacitance of 20pF. These signals are delayed by up to 80ns from the Z80A address bus timing, so they may not be stable as /MREQ goes low.
A15	b9	
A16	b26	
A17	a27	
A18	b27	
A19	a28	
A20	b28	
A21	a29	
/RD	a3	Active low read strobe. Used to gate output buffers of memory or I/O devices onto the data bus. Can drive 1 LS load with a maximum capacitance of 10pF. Timing as Z80A /RD.
/WR	b2	Active low write strobe. Used to strobe valid data on the bus into external memory or I/O. Can drive 3 LS loads with a maximum capacitance of 20pF. Timing as Z80A /WR.
/MREQ	a5	Active low memory request. Indicates that the address bus holds a valid address for a memory read or write operation. Can drive 3 LS loads with a maximum capacitance of 20pF. Timing as Z80A /MREQ.

SIGNAL	PIN	DESCRIPTION
/IORQ	b3	Active low input/output request. Indicates that A0-A7 hold a valid address for an input or output operation. Can drive 4 LS loads with a maximum capacitance of 30pF. Timing as Z80A /IORQ.
/RFSH	a2	Active low refresh signal. Indicates that A0-A6 of the address bus hold a 7-bit refresh address and that the current /MREQ may be used to do a refresh cycle to all external dynamic memories. Can drive 4 LS loads with a maximum capacitance of 35pF. Timing as Z80A /RFSH.
/M1	a20	Active low signal indicates that the current machine cycle is the op-code fetch of an instruction execution. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle. Can drive 4 LS loads with a maximum capacitance of 30pF. Timing as Z80A /M1.
/RESET	a18	Active low output. Gives 1mS pulse synchronised to the falling edge of /M1 when reset button pressed or when power first applied to computer. Can drive 2 LS loads with a maximum capacitance of 15pF.
/INT	b18	Active low interrupt input. Must be driven with an open-collector device capable of sinking 2.5mA.
/NMI	b5	Active low non-maskable interrupt input. Must be driven with an open-collector device capable of sinking 2.5mA.
/WAIT	a19	Active low signal indicates that an external device is not ready for a data transfer. Must be driven with an open-collector device capable of sinking 2.5mA. Timing as Z80A /WAIT.
PHI	a22	Z80A clock signal. Nominally 4MHz, with breaks of up to 1.2uS when Z80A accesses Nick chip. This signal should only be used for synchronising external events to the cpu, not as a 4MHz clock. Can drive 1 LS load with a maximum capacitance of 10pF.
1MHz	a21	1MHz 50% duty cycle clock output. Can drive 3 LS loads with a maximum capacitance of 30pf.

SIGNAL	PIN	DESCRIPTION
8MHz	a23	8MHz clock output. Can drive 4 LS loads with a maximum capacitance of 30pF.
14MHz	b29	Video dot clock. Varies between 14MHz and 14.25MHz depending on TV colour modulation system. This signal contains frequency jitter at half horizontal line frequency. Can drive 1 ALS load with a maximum capacitance of 8pF.
/HSYNC	a32	Active low horizontal picture sync output. Can drive 10 LS loads.
/VSYNC	b30	Active low vertical picture sync output. Can drive 10 LS loads.
EC0 EC1 EC2 EC3	a24 b24 a25 b25	External colour inputs to Nick palette. Driving device must be capable of sinking 8mA. Only one expansion card may drive these inputs.
/EXTC	a26	Active low external colour enable signal. When active, inputs EC0-3 are output to video display through colour palette of Nick chip. See Nick programming description for details of priority. Driving device must be capable of sinking 8mA. Only one expansion card may drive this input.
L.H.AUDIO	b1	Left-hand channel audio input. 3V p.t.p. into 1k5 for full output.
R.H.AUDIO	a1	Right-hand channel audio input. 3V p.t.p. into 1k5 for full output.
/EXP	b31	Active low expansion data buffer enable. Not connected on computer. This line must be pulled low by an open-collector device in any addressed expansion card to enable data buffers on motherboard. Driving device must be capable of sinking 6mA.
GND	a30,a31 b19,b20 b21,b22 b23,b32	Supply return and logic ground.(8 pins).
+5V	a4,b4	These pins are not connected on computer but are used for +5 volt supply on the motherboard.

SIGNAL	PIN	DESCRIPTION
+9V	a33,b33	9 volt dc supply (2 pins). These pins are for test use only. No power is available for external use. Flexible adaptor cable must leave these pins unconnected at the computer end and connected to GND at the expansion module / motherboard end. Expansion modules use these lines as extra ground pins.

Bus Timing.
Refer to drg A3PER1.

SIGNAL	REF	PARAMETER	MIN	MAX
PHI	1	Clock period.	250nS	1500nS
	2	Clock high pulse width.	110nS	1380nS
	3	Clock low pulse width.	110nS	1380nS
A0-A13	4	Low address output delay.		110nS
	5	Low address stable prior to /MREQ (memory cycle).	60nS	
	6	Low address stable prior to /IORQ, /RD or /WR (IO cycle).	180nS	
	7	Low address stable from /RD,/WR, /IORQ or /MREQ.	75nS	
A14-A21	8	Delay from low address stable to high address stable.		80nS
D0-D7	9	Data output delay.		150nS
	10	Delay to float during write cycle.		90nS
	11	Data setup time, M1 cycle.	35nS	
	12	Data setup time, M2-M5 cycle.	50nS	
	13	Data stable prior to /WR (memory cycle).	80nS	
	14	Data stable prior to /WR (IO cycle).	-45nS	
	15	Data stable from /WR.	55nS	
	16	Input hold time.	0nS	
/MREQ	17	/MREQ delay from falling edge of clock, /MREQ low.	20nS	85nS
	18	/MREQ delay from rising edge of clock, /MREQ high.		85nS
	19	/MREQ delay from falling edge of clock, /MREQ high.		85nS
	20	Pulse width, /MREQ low.	220nS	
	21	Pulse width, /MREQ high.	105nS	
/IORQ	22	/IORQ delay from rising edge of clock, /IORQ low.		75nS
	23	/IORQ delay from falling edge of clock, /IORQ low.		85nS
	24	/IORQ delay from rising edge of clock, /IORQ high.		85nS
	25	/IORQ delay from falling edge of clock, /IORQ high.		85nS

SIGNAL	REF	PARAMETER	MIN	MAX
/RD	26	/RD delay from rising edge of clock, /RD low.		85nS
	27	/RD delay from falling edge of clock. /RD low.		95nS
	28	/RD delay from rising edge of clock, /RD high.		85nS
	29	/RD delay from falling edge of clock, /RD high.		85nS
/WR	30	/WR delay from rising edge of clock, /WR low.		65nS
	31	/WR delay from falling edge of clock, /WR low.		80nS
	32	/WR delay from falling edge of clock, /WR high.		80nS
	33	Pulse width, /WR low.	220nS	
/M1	34	/M1 delay from rising edge of clock, /M1 low.		100nS
	35	/M1 delay from rising edge of clock, /M1 high.		100nS
/RFSH	36	/RFSH delay from rising edge of clock, /RFSH low.		130nS
	37	/RFSH delay from rising edge of clock, /RFSH high.		120nS
/WAIT	38	/WAIT setup time to falling edge of clock.	70nS	
	39	/WAIT hold time from falling edge of clock.	0nS	
/INT	40	/INT setup time to rising edge of clock.	80nS	
	41	/INT hold time from rising edge of clock.	0nS	
/NMI	42	Pulse width, /NMI low.	80nS	
	43	/M1 stable prior to /IORQ (interrupt acknowledge).	560nS	

The above timings assume maximum load on the expansion bus, cartridge with 2 roms fitted, and internal 64k ram expansion board (128k version).

Note that the Dave chip inserts one wait state into each M1 cycle but this may be disabled by software. The Z80A also inserts wait states into IO accesses and interrupt acknowledge cycles.