DOCUMENT:	DPC12	CONFIDENTIAL
PROJECT:	DPC	
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SIGNAL DEFINITIONS

/RES (EXTERNAL INPUT). Master reset for chip is guaranteed low for several mS.

14M (EXTERNAL INPUT). The master video clock signal. This is supplied externally and will vary between 14.1 and 14.4MHz.

T-BUS

T0,T1,T2,T3,T4,T5,T6,T7
Taps on a twisted ring driven by the 14MHz signal.
/T0,/T1,/T2,/T3,/T4,/T5,/T6,/T7
Complements of the above.

/VRAS (EXTERNAL OUTPUT). The row address strobe for video dynamic RAM.
VMUX (EXTERNAL OUTPUT). The select for external 74LS158 address multiplexers.
/VCAS (EXTERNAL OUTPUT). The column address strobe for video dynamic RAM.
/VW (EXTERNAL OUTPUT). The write control for the video dynamic RAM.
/ACCESS (EXTERNAL OUTPUT). A signal which allows the Z80 access to the video RAM buses.

/UL1 A signal active low in the first 5 14MHz clocks of a memory cycle which is used by the VDC to window an access of the dynamic RAM.
/UL2 A signal active low for the next 5 clocks of the 14MHz video clock which is used by the VDC to window a second access of the video RAM.
/Z80 A signal active low for the next 6 14MHz clocks which windows the time during which the Z80 may access the video RAM or write to the VDC registers.
/ULA The complement of /Z80 which is low when /UL1 or /UL2 are low.

/LOAD1 A signal which goes low shortly after /ULA goes active which may be used to cause a load of the pixel shift register. It clocks on the negative edge of the 14MHz clock.
/LOAD2 Similar to /LOAD1 but occuring 8 clocks of the 14MHz after /LOAD1.
/LOAD1,/LOAD2
Complements of the above signals.

PIXCLK1 The original 14M used to clock the pixel shift register in the highest resolution pixel modes.
PIXCLK2 Half the frequency of PIXCLK1 phased (by /CRST at the start of each sscanline)to correspond to the /LOAD1 and /LOAD2 signals allowing the shift register to clock out at half the resolution of PIXCLK1.
PIXCLK3 As above but quarter the frequency of PIXCLK1.
PIXCLK4 As above but one eighth the frequency of PIXCLK1.

PIXCLK The actual pixel shift register clock (multiplexed from PIXCLK1 to PIXCLK4).
PIXLOAD The actual /LOAD control signal for the pixel shift register.

/INCPIX An active low signal which is used to give an extra clock to the LD1 data pointer in the PIXEL mode (while the display is active).

/CRST A signal which goes low for a memory cycle (/UL1+/UL2+/Z80) at the end of each video scanline (63.7uS for the NTSC machine). This is used to reset a divide by 57 ripple counter clocking off /ULA.

C-BUS

C0,C1,C2,C3,C4,C5
The outputs of the ripple counter which count the memory cycles across the screen. A ripple counter is alright because the count values are used in conjunction with T7 ie: after they have stabilised.
/C0,/C1,/C2,/C3,/C4,/C5
Complements of the above.

LP-BUS

/SC A signal which goes low when the scanline in modeline counter is loaded from the line parameter table in RAM.

/MB A signal which goes low when the Modebyte register is loaded.

/LM A signal which goes low when the left margin register is loaded.

/RM A signal which goes low when the right margin register is loaded.

/LD1L A signal which goes low when the low 8 bits of the LD1 data pointer is loaded.

/LD1H A signal which goes low when the high eight bits of the LD1 data pointer is loaded.

/LD2L A signal which goes low when the low 8 bits of the LD2 data pointer is loaded.

/LD2H A signal which goes low when the high eight bits of the LD2 data pointer is loaded.

/COL0,/COL1,/COL2,/COL3,/COL4,/COL5,/COL6,/COL7
Signals which go low to load the various logical colours from the line parameter table in RAM.

/UPARMS A signal which goes low when the line parameters (/SC..../COL7) are being loaded from the line parameter table in video RAM.

/RFSH' A signal which goes low while refresh addresses are being generated for the video dynamic RAM.

/VUL1 A signal which goes low during the /UL1 time (ie: first VDC access of video RAM) if neither line parameter addresses or refresh addresses are being output.

/VUL2 A signal which goes low during the /UL2 time (ie: second VDC access of video RAM) if neither line parameter addresses or refresh addresses are being output.

/ENLD1 A signal which goes low when the LD1 line data pointer can output an address.

LD1CLK A signal which clocks the LD1 data pointer while the display is active. LD1 is clocked twice per active memory cycle in the PIXEL mode but only once per active memory cycle in the other modes.

/LD1LD A low going signal which causes the LD1 counter to reload from the line parameter table. It is reloaded on every scanline in the ATTR, CH256, CH128 and CH64 modes. It is reloaded only on the modeline in PIXEL and LPIXEL modes.

/ENLD2 A signal which goes low when the LD2 line data pointer can output an address.

LD2CLK A signal which clocks the LD2 data pointer at the beginning of each scanline in the CH256, CH128 and CH64 modes and in every active memory cycle of the ATTR mode. It is not active in the PIXEL and LPIXEL modes.

/LD2LD A low going signal which causes the LD2 counter to reload from the line parameter table at the start of each modeline.

/ML A signal which is active low during a modeline.

/VIWR An active low signal formed when the Z80 is writing to the internal registers of the VDC.

LPL An active high signal formed when the Z80 is writing to the register holding A4-A11 of the line parameter table base address.

LPH An active high signal formed when the Z80 is writing to the register which holds A12-A15 of the line parameter table base address (as well as special control output to for the startup loading of the line parameter block counter).

BORDER An active high signal formed when the Z80 is writing to the register which defines the border colour of the display.

FIXBIAS An active high signal formed when the Z80 is writing to the register which defines the fixed bias of logical colours 8 to 15, the VC1 (colour kill) output and the PRIORITY signals.

VC1 (EXTERNAL OUTPUT). A general purpose output but used to kill the colour subcarrier oscillator for B&W TVs.

PRIOR1,PRIOR0
Signals defining the priority on the screen of external colour signals over the display generated by the VDC circuits.