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AUTHOR:	Nick Toop	
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TO:	RM,BT,RW,JC,AMI	SOFTWARE LTD

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SIGNAL DEFINITIONS

/RES (EXTERNAL INPUT). Master reset for chip is guaranteed low for several mS.

14M (EXTERNAL INPUT). The master video clock signal. This is supplied externally and will vary between 14.1 and 14.4MHz.

T-BUS

T0,T1,T2,T3,T4,T5,T6,T7
Taps on a twisted ring driven by the 14MHz signal.
/T0,/T1,/T2,/T3,/T4,/T5,/T6,/T7
Complements of the above.

/VRAS (EXTERNAL OUTPUT). The row address strobe for video dynamic RAM.
VMUX (EXTERNAL OUTPUT). The select for external 74LS158 address multiplexers.
/VCAS (EXTERNAL OUTPUT). The column address strobe for video dynamic RAM.
/VW (EXTERNAL OUTPUT). The write control for the video dynamic RAM.
/ACCESS (EXTERNAL OUTPUT). A signal which allows the Z80 access to the video RAM buses.

/UL1 A signal active low in the first 5 14MHz clocks of a memory cycle which is used by the VDC to window an access of the dynamic RAM.
/UL2 A signal active low for the next 5 clocks of the 14MHz video clock which is used by the VDC to window a second access of the video RAM.
/Z80 A signal active low for the next 6 14MHz clocks which windows the time during which the Z80 may access the video RAM or write to the VDC registers.
/ULA The complement of /Z80 which is low when /UL1 or /UL2 are low.

/LOAD1 A signal which goes low shortly after /ULA goes active which may be used to cause a load of the pixel shift register. It clocks on the negative edge of the 14MHz clock.
/LOAD2 Similar to /LOAD1 but occuring 8 clocks of the 14MHz after /LOAD1.
/LOAD1,/LOAD2
Complements of the above signals.

PIXCLK1 The original 14M used to clock the pixel shift register in the highest resolution pixel modes.
PIXCLK2 Half the frequency of PIXCLK1 phased (by /CRST at the start of each sscanline)to correspond to the /LOAD1 and /LOAD2 signals allowing the shift register to clock out at half the resolution of PIXCLK1.
PIXCLK3 As above but quarter the frequency of PIXCLK1.
PIXCLK4 As above but one eighth the frequency of PIXCLK1.

PIXCLK The actual pixel shift register clock (multiplexed from PIXCLK1 to PIXCLK4).
PIXLOAD The actual /LOAD control signal for the pixel shift register.

/INCPIX An active low signal which is used to give an extra clock to the LD1 data pointer in the PIXEL mode (while the display is active).

/CRST A signal which goes low for a memory cycle (/UL1+/UL2+/Z80) at the end of each video scanline (63.7uS for the NTSC machine). This is used to reset a divide by 57 ripple counter clocking off /ULA.

C-BUS

C0,C1,C2,C3,C4,C5
The outputs of the ripple counter which count the memory cycles across the screen. A ripple counter is alright because the count values are used in conjunction with T7 ie: after they have stabilised.
/C0,/C1,/C2,/C3,/C4,/C5
Complements of the above.

LP-BUS

/SC A signal which goes low when the scanline in modeline counter is loaded from the line parameter table in RAM.

/MB A signal which goes low when the Modebyte register is loaded.

/LM A signal which goes low when the left margin register is loaded.

/RM A signal which goes low when the right margin register is loaded.

/LD1L A signal which goes low when the low 8 bits of the LD1 data pointer is loaded.

/LD1H A signal which goes low when the high eight bits of the LD1 data pointer is loaded.

/LD2L A signal which goes low when the low 8 bits of the LD2 data pointer is loaded.

/LD2H A signal which goes low when the high eight bits of the LD2 data pointer is loaded.

/COL0,/COL1,/COL2,/COL3,/COL4,/COL5,/COL6,/COL7
Signals which go low to load the various logical colours from the line parameter table in RAM.

/UPARMS A signal which goes low when the line parameters (/SC..../COL7) are being loaded from the line parameter table in video RAM.

/RFSH' A signal which goes low while refresh addresses are being generated for the video dynamic RAM.

/VUL1 A signal which goes low during the /UL1 time (ie: first VDC access of video RAM) if neither line parameter addresses or refresh addresses are being output.

/VUL2 A signal which goes low during the /UL2 time (ie: second VDC access of video RAM) if neither line parameter addresses or refresh addresses are being output.

/ENLD1 A signal which goes low when the LD1 line data pointer can output an address.

LD1CLK A signal which clocks the LD1 data pointer while the display is active. LD1 is clocked twice per active memory cycle in the PIXEL mode but only once per active memory cycle in the other modes.

/LD1LD A low going signal which causes the LD1 counter to reload from the line parameter table. It is reloaded on every scanline in the ATTR, CH256, CH128 and CH64 modes. It is reloaded only on the modeline in PIXEL and LPIXEL modes.

/ENLD2 A signal which goes low when the LD2 line data pointer can output an address.

LD2CLK A signal which clocks the LD2 data pointer at the beginning of each scanline in the CH256, CH128 and CH64 modes and in every active memory cycle of the ATTR mode. It is not active in the PIXEL and LPIXEL modes.

/LD2LD A low going signal which causes the LD2 counter to reload from the line parameter table at the start of each modeline.

/ML A signal which is active low during a modeline.

/VIWR An active low signal formed when the Z80 is writing to the internal registers of the VDC.

LPL An active high signal formed when the Z80 is writing to the register holding A4-A11 of the line parameter table base address.

LPH An active high signal formed when the Z80 is writing to the register which holds A12-A15 of the line parameter table base address (as well as special control output to for the startup loading of the line parameter block counter).

BORDER An active high signal formed when the Z80 is writing to the register which defines the border colour of the display.

FIXBIAS An active high signal formed when the Z80 is writing to the register which defines the fixed bias of logical colours 8 to 15, the VC1 (colour kill) output and the PRIORITY signals.

VC1 (EXTERNAL OUTPUT). A general purpose output but used to kill the colour subcarrier oscillator for B&W TVs.

PRIOR1,PRIOR0
Signals defining the priority on the screen of external colour signals over the display generated by the VDC circuits.

/HSYNC (EXTERNAL OUTPUT). The horizontal sync pulse for the video display which goes low for 4 memory cycles (4.47uS) at the beginning of a video scanline. It clocked by T7 and derives from the column ripple counter outputs.

/BURST (EXTERNAL OUTPUT). The burst strobe for the video colour modulator which goes low for 4 memory cycles (4.47uS) 2 memory cycles (2.23uS) after the /HSYNC pulse. This is inhibited when the VSYNC mode is active ie: when /VSYN is low.

/BLNK (EXTERNAL OUTPUT). A signal which goes low when there is no display on a line ie: to left and right of the screen. This defines the limits of the BORDER colour rather than the active display. It is permanently low in the VSYNC mode which uses margin information to define the position of the vertical sync pulse.

/VSYNC (EXTERNAL OUTPUT). The vertical sync pulse for the video display device which is derived from the display margin registers LM and RM in the VSYNC mode (/VSYN low). Since it derives from the display margine registers it can be made to go active (low) halfway through the video scanline for an interlaced display frame.

RELOAD A signal from the MODEBYTE register which causes the line parameter pointer/counter to be reloaded from the line parameter base registers. This will normally be made to active at the end of each video frame or after 2 video frames if the display is interlaced.

SM2,SM1,SM0
3 bits of the MODEBYTE register which define the screen operation mode for the modeline. It is decoded to the following...

/VSYN A signal which goes low if the MODEBYTE register defines VSYNC mode.
/PIXEL A signal which goes low if the MODEBYTE register defines PIXEL mode.
/ATTR A signal which goes low if the MODEBYTE register defines ATTR mode.
/CH256 A signal which goes low if the MODEBYTE register defines CH256 mode.
/CH128 A signal which goes low if the MODEBYTE register defines CH128 mode.
/CH64 A signal which goes low if the MODEBYTE register defines CH64 mode.
/LPIXEL A signal which goes low if the MODEBYTE register defines LPIXEL mode.

CM1,CM0 Signals from the MODEBYTE register which define the colour mode of the screen ie: 00 for 2C 2 colour mode
01 for 4C 4 colour mode
10 for 16C 16 colour mode
11 for 256C 256 colour mode

/VIRQ (EXTERNAL OUTPUT) from a bit in the MODEBYTE used to generate a video interrupt FOR THE Z80.

VRES A signal from the MODEBYTE register which causes the LD1 and LD2 data pointers to be reloaded at the start of each scanline of the current modeline. This causes the scanline to be repeated for the duration of the modeline. It is mainly included as a test mode but does allow for exfficient use of memory in low resolution PIXEL modes.

UA0,UA1,UA2,UA3,UA4,UA5,UA6,UA7
(EXTERNAL INPUT/OUTPUT) Bidirectional connection to low bits of video address bus. The VDC will output addresses on these pins during the /ULA time and input an address at the /Z80 time. The input address may be used to write the VDC registers.

UA8,UA9,UA10,UA11,UA12,UA13,UA14,UA15
(EXTERNAL OUTPUT). The VDC will output address bits on these pins during the /ULA time.

A-BUS

A0,A1,A2,A3,A4,A5,A6,A7,A8,A9,A10,A11,A12,A13,A14,A15
The buffered internal version of the UA address bits. Note that only A0,A1 need to be bidirectional.

UD0,UD1,UD2,UD3,UD4,UD5,UD6,UD7
(EXTERNAL INPUTS). During the /ULA time the VDC reads data from

the video RAM on these pins. Data for the internal registers on the VDC may be presented at the /Z80 time.

D-BUS

D0,D1,D2,D3,D4,D5,D6,D7
The buffered databus. This may contain information for the VDC registers, from the line parameter table, and from display data tables.

L-BUS

L0,L1,L2,L3,L4,L5,L6,L7,L8,L9
Some of the outputs of the LD1 data pointer counter which may be used to generate a character font address in conjunction with the contents of bufferi (the index of the character).

/ACTIVE A signal clocked by T7 which goes active low between the limits defined by the contents of the LM and RM (left and right margin) registers. It is used to delimit the actual display (although this clocks out on the screen a bit later) or to form the /VSYNC pulse in the VSYNC mode.

S-BUS

S0,S1,S2,S3,S4,S5,S6,S7
The screen data bus. Basically the data to be loaded into the pixel shift register but also the route whereby an index in bufferi is used to generate a pointer into the character font.
/SDATA Low when there is data on the S-BUS corresponding to active display.

S'-BUS

S0',S1',S2',S3',S4',S5',S6',S7'
In PIXEL mode this is a delayed version of the S-BUS but otherwise it is the same as the S-BUS. The delay is necessary because without it PIXEL mode data would appear on the screen before corresponding character data.

SA-BUS

SA,SB,SC,SD,SE,SF,SG,SH
The outputs of the pixel shift register. In 2C and ATTR mode SH defines the colour of the screen. In 4C mode SD and SH define the colour of a pixel. In 16C mode SB,SD,SF,SH and in 256C mode SA,SB,SC,SD,SE,SF,SG,SH.

P-BUS

P0,P1,P2,P3
The palette bus. The basic operation of the machine is that a 4 bit value on the P-BUS define on of 16 logical colours. The first 8 logical colours COL0,COL1,.....COL7 are define from the line parameter table at the start of each scanline and the last 8 (FIXEDBIAS) colours have RGB components defined by their low 3 bits and an overall colour bias defined bu the conents of the FIXBIAS register. However, in order to allow prioritisation with regard to an external signal on the external colour inputs the P-BUS routes through a multiplexer to form the Q-BUS which is the same as the P-BUS if no external signal is supplied.
NB: The 256C colour mode bypasses the palette bus unless an external colour signal is supplied in which case a 16C mode is forced.

EC0,EC1,EC2,EC3
(EXTERNAL INPUTS). An alternative value for the palette colour supplied externally (eg: by SPRITE generation circuits). This is ignored unless /EXTC is low. If /EXTC is low the EC input will override the P-BUS signal on the Q-BUS if the priority determined by PRIOR1 and PRIOR0 is sufficient.
/EXTC (EXTERNAL INPUT). Low if an external colour input is being supplied.

Q-BUS

Q0,Q1,Q2,Q3
The multiplexed palette bus. If an external colour is supplied on EC0,..EC3 this may reflect the the EC inputs rather than the P bus. The Q-BUS selects one of the the 8 logical colour registers in the palette or one of 8 FIXBIAS colours.

PC'-BUS

PC0',PC1',PC2',PC3',PC4',PC5',PC6',PC7'
The 8-bit output of the PALETTE, BORDER or 256C mode buffer. This is clocked by a final flipflop at 14MHz to form the PC-BUS.

PC-BUS

PC0,PC1,PC2,PC3,PC4,PC5,PC6,PC7
(EXTERNAL). These outputs (changing at 7MHz) define the current physical colour on the screen.

RED = (PC0,PC3,PC6)
GREEN= (PC1,PC4,PC7)
BLUE = (PC2,PC5)

MSBALT An output from the LM register. If set it causes S7' to be treated specially (except in the ATTR mode). The pixel shift register is loaded as if S0' is 0 and S0' causes P2 of the palette bus to be set if S0' is set. (Normally used to highlight characters if the PIXEL mode is used for 84 column text.)

LSBALT An output from the LM register. If set it causes S0' to be treated specially (except in the ATTR mode). The pixel shift register is loaded as if S7' is 0 and S7' causes P1 of the palette bus to be set if S7' is set. (Normally used to highlight characters if the PIXEL mode is used for 84 column text.)

ALTIND1 An output from the RM register. If set it causes P1 to be set if the MSB of the character index is set. (Normally only use in CH256, CH128 and CH64 modes.)

ALTIND0 An output from the RM register. If set it causes P2 of the palette o be set if the next to MSB of the character index is set. (Normally only use in 2C colour mode of CH256, CH128 and CH64 modes.)

/CPAL A signal which is low if a palette mode is active ie: 2C, 4C or 16C colour with PIXEL,CH256,CH128,CH64 or LPIXEL.

/OVER A signal which is active low when and external colour is overwriting the internally generated display.

NOVER The complement of /OVER

/NCOL A signal active low for the 2C, 4C and 16C modes.

/ATTROK A signal active low when ATTR mode is selected and there is no external colour overwrite.

/PICT A signal which is active low when pixel data is clocking out on the screen.

PICT The complement of /PICT

/UACT Active low when /ULA is low and /ACTIVE is low.

THEORY OF OPERATION

All the video timing derives from the 14M input. The 8MHz input is only used by the Z80 clock generation circuitry which should be viewed as a separate circuit. The 14MHz is the pixel dot rate in the highest resolution pixel modes and is used to define memory access "slots" (see DPC11.DOC).

In the following part of the document timings relate to the NTSC running of the machine. All flipflops and counters are assumed to trigger on positive clock edges unless the contrary is specifically indicated.

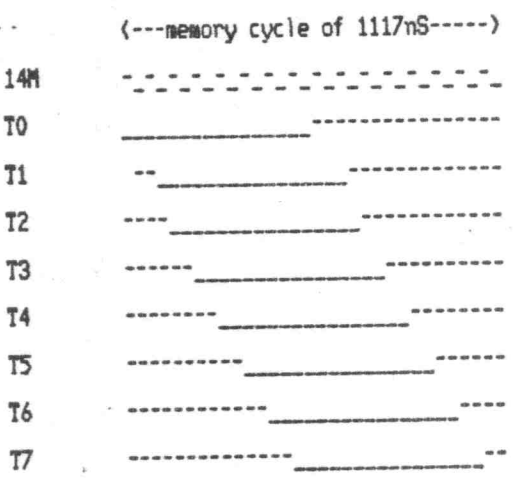
Z80 CLOCK STRETCH

This should be viewed as a separate subunit and does not affect the rest of the VDC other than it generates RESTART which is an internal signal of the VDC.
See other documents ie: DPC09 or DPC08.

14M RING & PIXEL CLOCK

The 14M drives an eight stage twisted ring Q79 ,Q80 which provides 16 differently phased 0.89MHz signals (T0, T1, T2,....T7, /T0, /T1,..../T7) on the T-BUS. The twisted ring is reset through Q121(4,5,6) by an external /RESET pulse which has a guaranteed duration of several mS. Nevertheless some sort of Schmitt action is probably desirable to prevent 1/2 states.

A MEMORY CYCLE

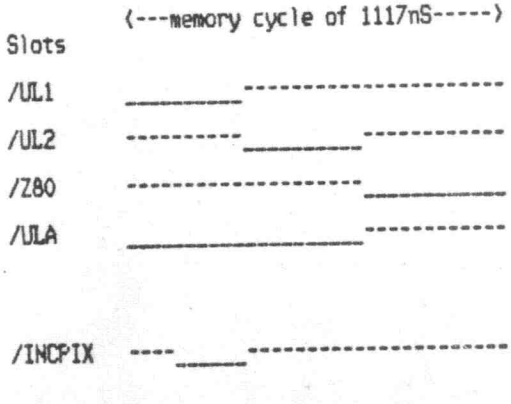


NB: - is about 36nS

The T-BUS signals are used to generate the "slots" of a memory cycle ie:

/UL1 from /T0 and T5 by Q115(4,5,6)
/UL2 from /T5 and T2 by Q115(10,9,8)
/Z80 from T0 and T2 by Q115(1,2,3)
/ULA from T0 and T2 by Q114(10,9,8) {use a NOR here?}

The VDC uses the video address and data buses in the /UL1 and /UL2 times and the Z80 can use the video address and data buses in the /Z80 time. Note that /ULA is low if either /UL1 or /UL2 are low and that it is the complement of /Z80.



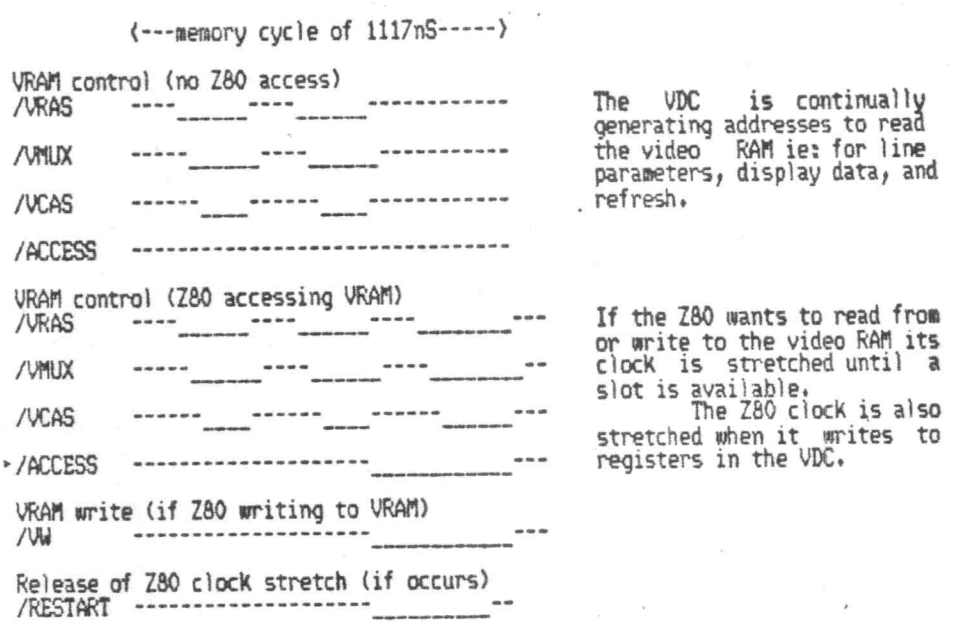
Video address bus use is split up into slots. /UL1 is used to get data for buffer#1 or the line parameters SC,LM, LD1L,LD2L,COL0,COL2,COL4,COL6 or a refresh address. /UL2 is used to get data for buffer#2 or the line parameters MB,RM, LD1H,LD2H,COL1,COL3,COL5,COL7 or a refresh address. /Z80 is available for use by the Z80 to access video RAM or write to a video register. /INCPIX gives the LD1 counter an extra count in the PIXEL mode.

The control strobes for the video RAM are derived as follows:

/VRAS from /T2 and T5 by Q116(10,9,8) in the /UL1 slot
from T2 and /T7 by Q116(13,12,11) in the /UL2 slot
from /T0 and /T4 by Q117(13,12,11) and Q117(10,9,8) in the /Z80 slot

VMUX by delaying /VRAS 36nS by clocking it on the other edge of 14M using Q86(2,3,5)

/VCAS from /T3 and T5 by Q121(1,2,3) in the /UL1 slot
from T0 and /T2 by Q116(4,5,6) in the /UL2 slot
from /T0 and /T5 by Q117(13,12,11) and Q118(1,2,3) in the /Z80 slot.



The VDC is continually generating addresses to read the video RAM ie: for line parameters, display data, and refresh.

If the Z80 wants to read from or write to the video RAM its clock is stretched until a slot is available.
The Z80 clock is also stretched when it writes to registers in the VDC.

The control signals for the pixel shift register are derived as follows:

/PIXLOAD is derived from /LOAD1 and /LOAD2 in PIXEL mode and from just /LOAD1 in other modes using Q90(13,12,11) and Q106(13,12,11).

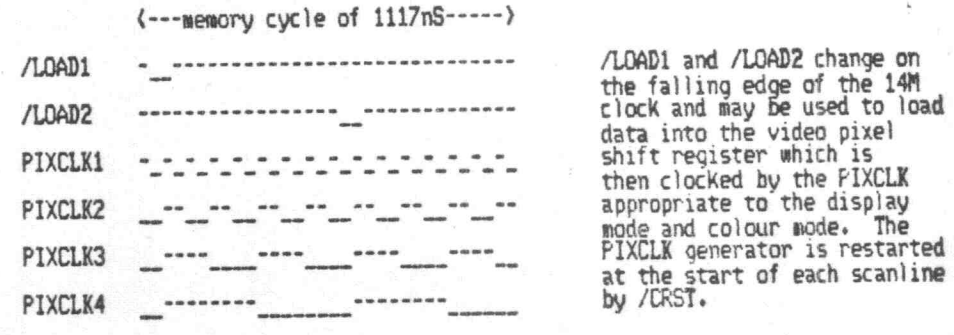
/LOAD1 from /T0 and T1 by Q113(13,12,11) delayed 36nS by Q81(2,3,5,6)

/LOAD2 from T0 and /T1 by Q116(1,2,3) delayed 36nS by Q81(12,11,9,8)

The pixel clock clocks the pixel shift register Q54,Q55 at a rate appropriate to the current screen mode and colour mode. This clock must be phased to when data is loaded into the shift register. This is done by dividing the 14M by a 4-bit synchronous counter Q77 which is reset at the start of each scanline bt /CRST. It is necessary that the various clocks are all in phase with the load signals /LOAD1 and /LOAD2. This phasing involves a gate delay kludge on the prototype. The clock rate used, PIXCLK, is selected by an 8 way multiplexer Q78 from the various outputs:

PIXCLK1	14MHz
PIXCLK2	7MHz
PIXCLK3	3.5MHz
PIXCLK4	0.88MHz

	2C	4C	16C	256C
PIXEL	14MHz	7MHz	3.5MHz	1.75MHz
ATTR	7MHz	-	-	-
CH256	7MHz	3.5MHz	1.75MHz	0.88MHz
CH128	7MHz	3.5MHz	1.75MHz	0.88MHz
CH64	7MHz	3.5MHz	1.75MHz	0.88MHz
LPIXEL	7MHz	3.5MHz	1.75MHz	0.88MHz



/LOAD1 and /LOAD2 change on the falling edge of the 14M clock and may be used to load data into the video pixel shift register which is then clocked by the PIXCLK appropriate to the display mode and colour mode. The PIXCLK generator is restarted at the start of each scanline by /CRST.

COLUMN COUNTER AND MARGIN CONTROL

There are 57 memory cycles in a video scanline. Each memory cycle can conveniently be thought of as defining a column on the screen. In the PIXEL mode 2 * 8 bits of information are loaded from memory in a memory cycle and these are clocked out as 16 pixels in the 2C colour mode (8 in 4C, 4 in 16C and 2 in 256C). In the CH256 mode a character index is found in memory and one row in the character font is clocked out as 8 pixels (in 2C mode). The active display (non-border colour) starts and ends on complete memory cycles although the actual clocking out on the display is delayed somewhat. The divide by 57 and generation of memory cycle numbers (C5,C4,C3,C2,C2,C0) is done by a ripple counter clocked off /ULA (Q72, Q73, Q74). When this reaches a count of 56 a /CRST pulse is generated on the negative going edge of /ULA (ie: by /Z80) using Q104(12,10,9,8) and Q75(2,3,5).
The user can define the left and right hand margins of his active display from values loaded into the left and right margin registers LM and RM (Q64 and Q65). The low six bits of each of these registers are compared against the current column using comparators Q65,Q66 and Q68,Q69. The outputs of these comparators are clocked by T7 (using Q70) when the column count is stable. The time between the left and right margin (Q110(1,2,3) and Q110(4,5,6)) is used in two ways (Q109(5,6) Q113(1,2,3) Q113(4,5,6)):

1) If /VSYN is low (VSYNC mode) it defines the /VSYNC signal. Note that if a right margin is given an impossible value (>57) the /VSYNC signal can be made to continue over several scanlines until a modeline with possible right margin appears. Also note that this makes it easy to start and end the /VSYNC pulse anywhere along a video scanline which makes interlace easy.

2) If /VSYN is high the output of Q110(6) becomes the /ACTIVE signal which detrmines the margins of the users display.

LINE PARAMETER GENERATOR

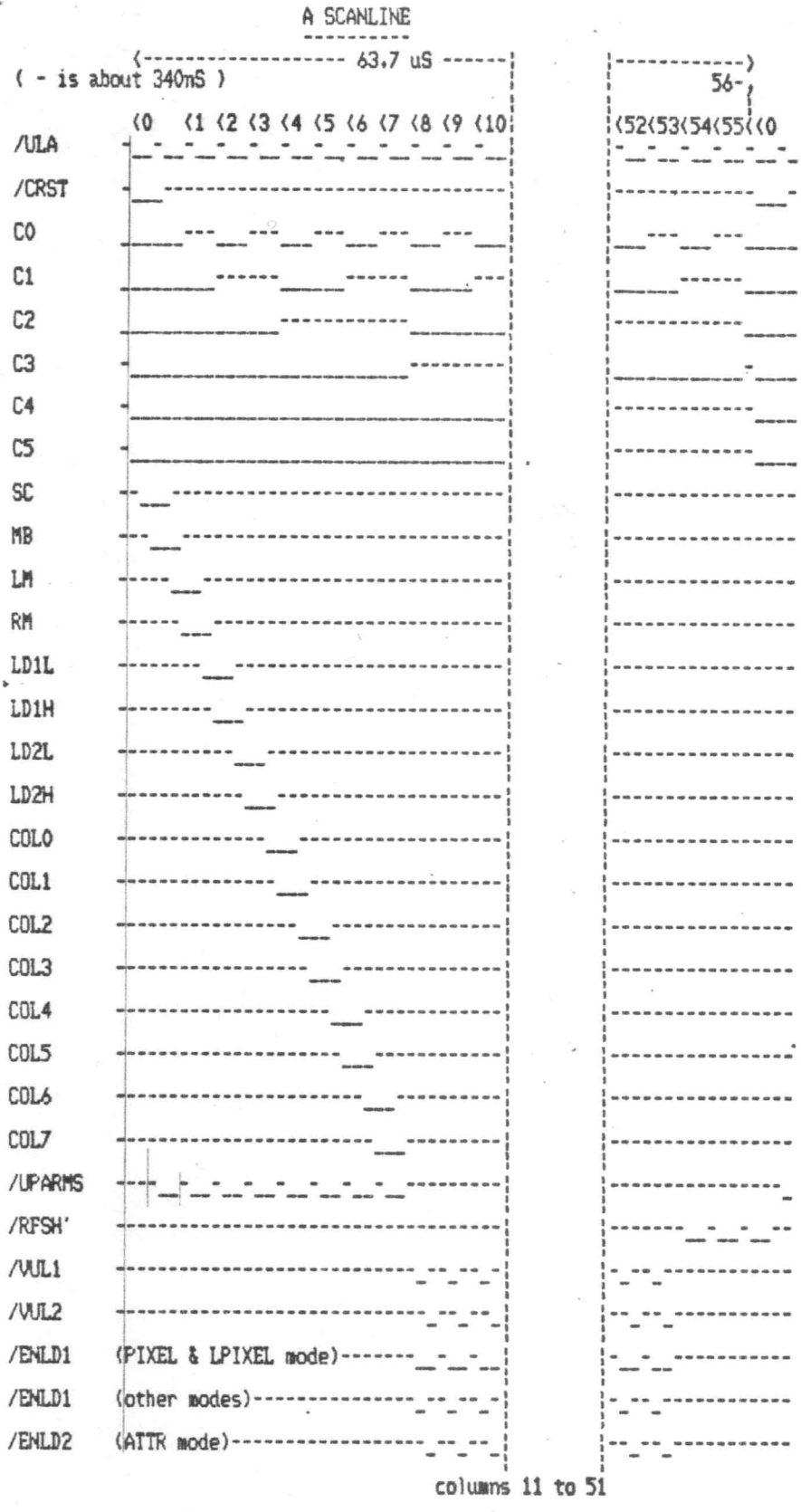
As described in other documents the nature of the display is determined by pointers and register values loaded by the Z80 into a section of video RAM. These values make up the line parameter table and can be located on any 16byte boundary of the 64K of video RAM. The table is made up of blocks of 16 bytes. The 12 bit pointer to the start of this table is stored in the line parameter base registers LPL and LPH (Q40 and Q41). This base value is loaded into the top 12 bits of the line parameter counter/pointer (Q42,Q43,Q44) whenever the RELOAD bit of the MODEBYTE is set or else if the user directly forces it by manipulation of the top bits of Q41.

The 12 bit line parameter block pointer is incremented after each modeline by the signal /MLRST which is low during /CRST time if /ML is low (Q98(1,2,3)). The /ML signal derives from the scanline in modeline counter Q47,Q48. This is clocked on every scanline by the /SC signal and reloaded on the line after it generates a carry (count FFH). The carry output is clocked by /COL0 to delay it to tne next line to form the active low signal /ML (Q86(12,11,8). This /ML signal is bracketed with /MB to form the load signal for the scanline counter (Q98(4,5,6)). { I dont think this bracketting with /MB is necessary!}

These 12 bits together with 4 low bits derived from /UL1 and C0,C1,C2 of the column counter (see below) make up a line parameter address. The line parameter addresses are output through Q43 and Q46 before each scanline while the signal /UPARMS is low.
Meanwhile the /CRST signal (a pulse generated at the start of each scanline) is shifting through two shift registers clocked off /UL1 and /UL2 respectively (Q34,Q35) to form low going strobes to latch in the data read from RAM at each line parameter address. These strobes: /SC, /MB, .../COL7 are used to clock in the data from addresses in the line parameter table pointed to by the line parameter pointer.
The /PARMS signal is derived from /C3,/C4,/C5 (Q105(1,2,4,6)) clocked by T7 (Q75(12,11,8)). /UPARMS is a similar signal gated with /Z80 (Q110(8,9,10)).

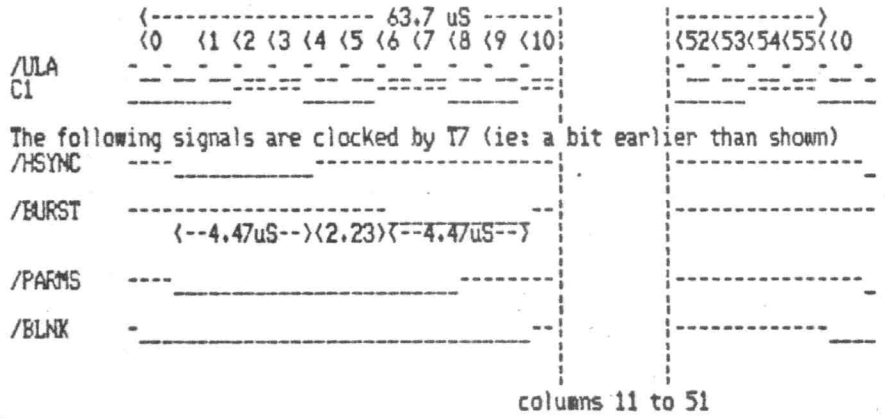
REFRESH ADDRESS GENERATOR

Since the addresses generated by VDC cannot be guaranteed to refresh dynamic RAM the VDC generates refresh addresses on A0-A7 at the end of each scanline. 6 new addresses are generated every 64uS so 8 bit refresh dynamic RAMs are refreshed every 2.7mS. The signal which determines when refresh addresses can be output (columns 54,55 and '56') is /RFSH'. This is generated from C1, C2, C4, C5, T7 using Q104(1,2,4,5,6), Q76, Q114(4,5,6), and Q117(1,2,3). This signal enables a tristate buffer onto A0-A7 (Q39). The actual refresh address has /UL1 as its LSB and the other 7 bits come from a 7 bit counter (Q38) which clocks off the positive going edge of /RFSH'.


A SCANLINE
63.7 uS
(- is about 340nS)
56
(0 (1 (2 (3 (4 (5 (6 (7 (8 (9 (10
(52(53(54(55((0
/ULA
/CRST
C0
C1
C2
C3
C4
C5
SC
MB
LM
RM
LD1L
LD1H
LD2L
LD2H
COL0
COL1
COL2
COL3
COL4
COL5
COL6
COL7
/UPARMS
/RFSH'
/VUL1
/VUL2
/ENLD1 (PIXEL & LPIXEL mode)
/ENLD1 (other modes)
/ENLD2 (ATTR mode)
columns 11 to 51

HSYNC, BURST, ETC:

The /HSYNC signal derives from /C2,/C3,/C4,/C5 gated by Q105(8,9,10,12,13), clocked by T7 using Q71(12,11,9).
The /BURST signal is the /HSYNC signal delayed through 2 cycles of C1 by Q71(2,3,4,5) and Q131(11,12,9). Note that /BURST is inhibited if /VSYN is low.
The /BLNK signal starts with /CRST and ends when C1 and /PARMS are high unless /VSYN is low in which case it is permanently low.
/PARMS is an output from Q75(9) ...see above.



NB: /BLNK is held permanently low while VSYNC mode is selected ie: /VSYN low.

The 0.89MHz signal is just T7 and the 3.58MHz is derived from 14M by a two stage ripple counter Q131.

The H/2 signal is derived from the /HSYNC pulses by Q125(11,12,8). It might be better to clock with /CRST.

IS THIS POSSIBLE?
Note that I would much prefer to replace the 0.89MHz and 3.58MHz outputs with a 4.433MHz input and a 7805Hz output.
The 7805Hz is 4.433MHz/568 and would be obtained as follows:

1) divide 4.433MHz by 4 using a 2 stage ripple counter
2) divide by 71 using a circuit like the 1/57 elsewhere
3) divide by 2 using a toggle flipflop to give 7805Hz.

THE MODEBYTE

One of the line parameters loaded at the start of a modeline is the MODEBYTE.

Bit 0 is inverted by Q132(9,8) to form the /RELOAD signal.
Bits (3,2,1) or SM2,SM1,SM0 are decoded by Q37 to define the screen mode ie: /VSYN, /PIXEL, /CH256, /CH128, /CH64, /UNUSED, /LPIXEL.
Bit 4 or VRES puts the VDC in a low resolution verical mode.
Bits (6,5) or CM1,CM0 define the colour mode.
Bit 7 or /VIRQ goes out of the chip to allow interrupts on a modeline.

The LD1 pointer and LD2 pointers are inhibited from outputting an address onto the A-BUS in the times when line parameters are being fetched, /PARMS, and when a refresh address is being generated, /RFSH'. Q89(3,4,5) and Q96(1,2,3 4,5,6) generate /VUL1 and /VUL2 from /UL1 and /UL2 at the times when the data pointers could use the /UL1 or /UL2 time slots.

LINE DATA POINTER #1

The #1 line data counter (Q22,Q23,Q24,Q25) is a 16 bit synchronous counter loaded at the start of the modeline in the PIXEL and LPIXEL modes and at the start of each scanline in the ATTR, CH256, CH128 and CH64 modes. It is incremented by LD1CLK which is generated from /ULA and /ACTIVE by Q113(10,9,8) for modes other than PIXEL. In the PIXEL mode an extra clocking pulse is required and this is derived from /INCPIX (Q123(8,9,10) gated in by Q113(13,12,11).
Since it must generate a stable address at /UL1 time and the address at /UL2 time in PIXEL mode the output is "pipelined" by the 2 octal flipflops Q26 and Q27. The LD1 data pointer points to character indices (cells) in the CH256, CH128 and CH64 modes, to attribute data in the ATTR mode, and to pixel data in the PIXEL and LPIXEL modes.
In LPIXEL and PIXEL modes Q96(13,12,11) and Q92(4,5,6) causes the LD1 pointer to be enabled (/ENLD1 low) in both the /VUL1 and /VUL2 times. For other modes it is only enabled at /VUL1 time. {NB: gate in /VSYN AS WELL?}

LINE DATA POINTER #2

The #2 line data counter (Q28,Q29,Q30,Q31) is a 16 bit synchronous counter loaded at the start of each modeline in the ATTR, CH256, CH128, and CH64 modes. It is not used in the PIXEL and LPIXEL modes. It is incremented by LD2CLK which is generated from /UACT (/ACTIVE and /ULA low) in the ATTR mode (Q90(10,9,8)) and from /CRST in other modes (Q132(1,2) Q90(4,5,6) Q92(1,2,3)).
The LD2 pointer increments for each active column in ATTR mode and for each scanline in other modes.
ATTR mode and on every new scanline of the modeline of CH256,CH128 and CH64 modes. Its output is enabled onto the internal address bus of the VDC through Q33 and Q34 at /VUL2 time by /ENLD2 if /ATTR is low (Q96(10,9,8)).

CHARACTER ADDRESS GENERATOR

In the CH256, CH128 and CH64 character modes the address put out by the LD1 data pointer in the /UL1 time is used to access the index of the character to be displayed. This index appears on the low bits of the address bus, A-BUS, at /VUL2 time while the higher bits define which line of which character font.
The precise way in which this character font pointer is form differs for the various character modes.

CH256 using Q91(1,2,3)
(L7,L6,L5,L4,L3,L2,L1,L0) -) (A15,A14,A13,A12,A11,A10,A9,A8) using Q16
(S7,S6,S5,S4) -) (A7,A6,A5,A4) using Q19(19)

CH128 using Q91(4,5,6)
(L8,L7,L6,L5,L4,L3,L2,L1) -) (A15,A14,A13,A12,A11,A10,A9,A8) using Q17
(L0,S6,S5,S4) -) (A7,A6,A5,A4) using Q20(1)

CH64 using Q91(10,9,8)
(L9,L8,L7,L6,L5,L4,L3,L2) -) (A15,A14,A13,A12,A11,A10,A9,A8) using Q18
(L1,L0,S5,S4) -) (A7,A6,A5,A4) using Q20(19)

CH256, CH128, CH64 using Q93(1,2,13,12) and Q91(13,12,11)
(S3,S2,S1,S0) -) (A3,A2,A1,A0) using Q19(1)

LINE DATA BUFFERS

The line data buffers store data pointed to by the line data pointers LD1 and LD2. Buffer #1 (Q57) is loaded at the end of a /VUL1 time and Buffer #2 (Q58) at the end of a /VUL2 time. They are enabled onto the S-BUS in turn. Buffer #1 drives the S-BUS when /VUL2 is low and /SDATA is low and Buffer #2 when /VUL2 is high and /SDATA is low using Q128(1,2) and Q127(1,2,3 4,5,6) {It would seem simpler to enable Buffer #1 off /UL2 and Buffer#2 of its inverse}.
The output of the line data buffers, the S-BUS, is used by the character address generator in the CH256,CH128,CH64 modes or becomes the S'-BUS which loads the pixel shift registers. The S'-BUS is the same as the S-BUS except in PIXEL mode for which it is delayed by the /PIXLOAD signal so that PIXEL and other modes starting at the same left hand margin will appear aligned on the screen.

SHIFT REGISTERS AND COLOUR MODE SELECTION

The S'-BUS is loaded into the pixel shift registers (Q54, Q55) on a positive going edge of PIXCLK when /PIXLOAD is low.

If MSBALT from the LM register (Q64) is high the data corresponding to S7' is loaded into the shift register Q55 as a 0 and the value of S7' is instead used to define the value of P2 on the palette (it is phased by Q56(12,11,9)).
Note that if ALTIND1 in the RM register (Q67) is high then the MSB of a character index has the same effect (Q61 and Q108(4,5,6)). This has the effect of mapping COL0,COL1,COL2,COL3 to COL4,COL5,COL6,COL7.

If LSBALT from the LM register (Q64) is high the data corresponding to S0' is loaded into the shift register Q55 as a 0 and the value of S0' is instead used to define the value of P1 on the palette bus, P-BUS, (it is phased by Q56(2,3,5). Note that if ALTIND0 in the RM register (Q67) is high then the next to MSB of a character index has the same effect (Q61 and Q108(4,5,6)). This has the effect of mapping COL0,COL1,COL4,COL5 to COL2,COL3,COL6,COL7.

The way in which the outputs of the pixel shift register control the palette bus or P-BUS depends on the colour mode selected:

CM1	CM0	MODE	
0	0	2C	2 colour mode uses SH to define P0
0	1	4C	4 colour mode uses SD and SH to define (P1,P0)
1	0	16C	16 colour mode uses SB,SF,SD and SH to define (P3-P0)
1	1	256C	256C mode sidesteps palette

The undefined bits of the palette bus are 0 unless one of the options mentioned above is in effect.
Q129(13,12,11) determines 2C mode from CM0 and CM1 ie: /2C low. In this mode Q106(3) will be low and since CM1 is also zero the outputs Q106(6) and Q106(8) will be zero and so P1, P2 and P3 on the palette will be zero unless one of the special options above is active at an input of Q98(9) or Q98(12).
If CM0 is high and CM1 is low SD will be enabled through to palette bit P1.
If both CM0 and CM1 are high SB,SF,SD and SH are enabled through onto the palette bus.

The active condition of option LSBALT comes through Q97(10,9,8) and ALTIND0 through Q107(10,9,8). These combine at Q108(1,2,3) and are delayed by Q56(2,3,5) which clocks the condition through at the same time as the pixel shift register is loaded. This can then take the P2 palette bit high (Q98(13,12,11)).

The active condition of option MSBALT comes through Q107(4,5,6) and ALTIND1 through Q107(13,12,11). These combine at Q108(4,5,6) and are delayed by Q56(12,11,9) which clocks the condition through at the same time as the pixel shift register is loaded. This can then take the P1 palette bit high (Q98(10,9,8)).

NB: In the above description note that signals reach the P-BUS though Q52(1) which is enabled if /NCOL is low. /NCOL is low if there is no external colour override (NOVER low) and ATTR mode is not selected (Q128(11,10), Q129(4,5,6)).

In the ATTR mode the attribute data loaded at /VUL1 time into Q57 and then Q61 is clocked into Q62 when the pixel information is loaded into the shift register. SH then controls output buffers Q63(1) and Q63(19) to define the 4 bit values of paper and ink on the palette bus.

NB: Note that signals are inhibited from reaching the palette bus unless /ATTROK is low. This is low if ATTR mode is selected and NOVER is low.

If CM0 and CM1 are high Q126(10,9,8) selects 256C mode (/256C low). This will turn the 256 colour buffer Q15 on if /PICT is low unless there is an external colour override (Q127(10,9,8 13,12,11)). In the event of such an override or if a colour mode other then 256C is selected the signal /CPAL (palette enable) is forced low while /PICT is low (Q128(5,6) Q130(1,2,3) Q129(10,9,8)).

EXTERNAL COLOUR PRIORITY

The gates Q132(11,10 13,12), Q100, Q89(10,9,8 13,12,11), Q128(13,12), Q99(5,6 9,8), Q102(1,2,3 4,5,6 10,9,8) and Q120(13,12,10,9,8) establish if the external colour on EC0-EC3 can override the internal colour generated by the VDC according to priority rules laid out in DPC11.DOC. If the external signal has priority it substitutes the EC-BUS for the P-BUS on the Q-BUS (Q53). If the current internal mode is 256C colour mode the mode is forced to 16C.

PALETTE REGISTERS, FIXBIAS COLOURS AND BORDER COLOUR

Active display is signalled by /PICT low. If the display uses the palette then /CPAL is low and if it is a 256 colour display /C256 is low.

If /CPAL is low and /PICT is low the 4-bit logical colour on the multiplexed palette bus Q-BUS is decoded to one of sixteen colours. Colours with Q3=0 ie: COL0,COL1,....COL7 are decoded by Q12 to enable one of the 8 palette colour registers Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8. If Q3=1 the tristate buffer Q14 is enabled which puts Q0,Q1,Q2 onto the low 3 bits of the PC'-BUS and the low 5 bit of the FIXBIAS register on the high 5 bits of the PC'-BUS. This forms the logical colours COL8,COL9,...COL15.

If /C256 is low and /PICT is low the SA-BUS is directly enabled onto the PC'-BUS to form one of 256 colours. Note that this is straight-through connection with much less delay than the palette route which must go through colour mode selection, onto the P-BUS, through the priority multiplexer to the Q-BUS and then be decoded to enable a palette register! Either this must all be done very fast or else phasing delays must be introduced into the /C256 path and border colour generator circuits.

If the display is not active and we are not in the blanking time (/BLNK low) then the border colour register Q9 is enabled onto the PC'-BUS. If /BLNK is active low a zero level is enabled onto the PC'-BUS by Q10. Note that simplifications could be made by consistent use of inversion.

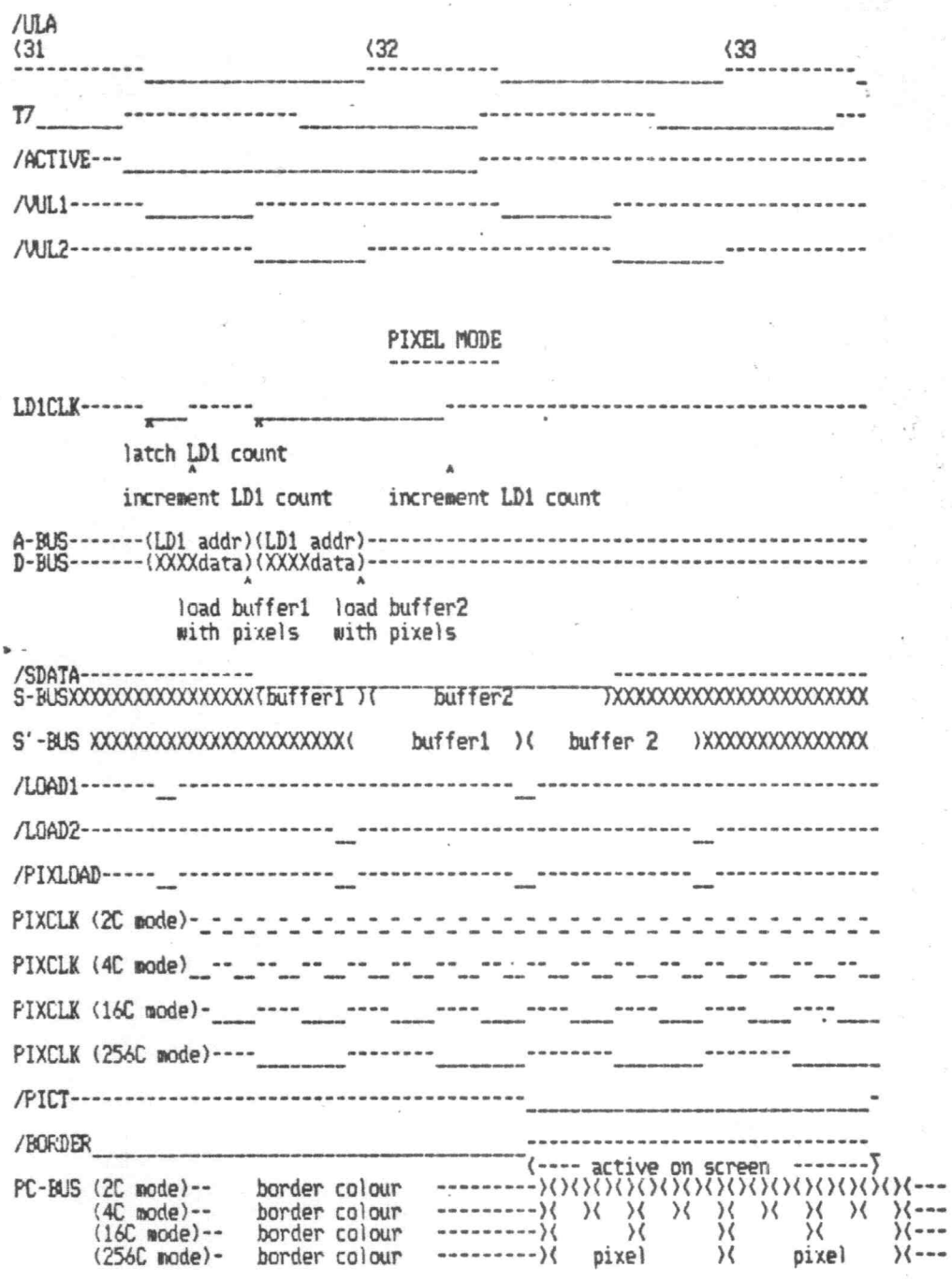
The value on the 8 bit PC'-BUS is clocked by Q11 at 14MHz to produce the final physical colour output on PC0,PC1,....PC7. It would be best if this were a high drive (5mA) CMOS bus but if we must use NMOS then it should be LSTTL.

MISC BITS

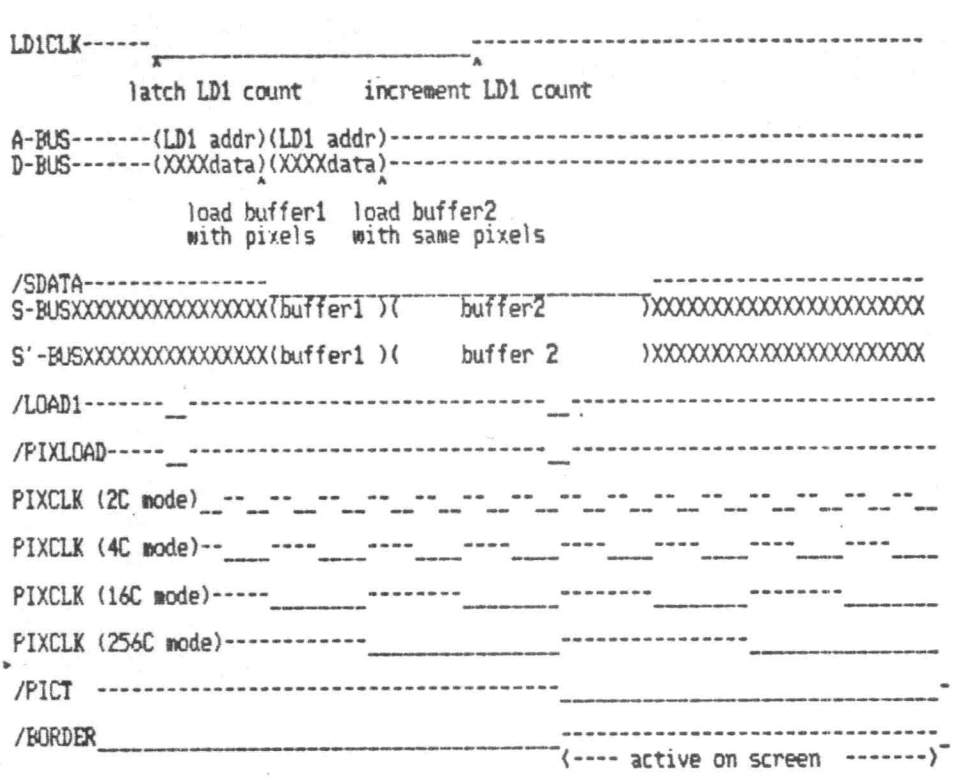
The address and data buses are buffered going into the chip. Since the VDC only reads from memory the data bus buffer (UD0-UD7) to D0-D7 is unidirectional (Q51). The low bits of the address bus are used to address internal registers of the VDC (LPL,LPH,FIXBIAS AND BORDER) and so the buffer on UA0 and UA1 needs to be bidirectional (Q49). In the VDC it might be simpler to have separate input buffers for UA0 and UA1 leading directly to the internal register decoder Q21. The high bits of the address bus UA8-UA15 are tristating outputs of the VDC (Q50).

The address decodes for the various registers of the VDC come from Q21 and Q88 (5,6 9,8 11,10 13,12). The enable for this decode is /VIWR which is active low when the Z80 is writing to an IO address in the range 080H to 08FH (/VIO low).

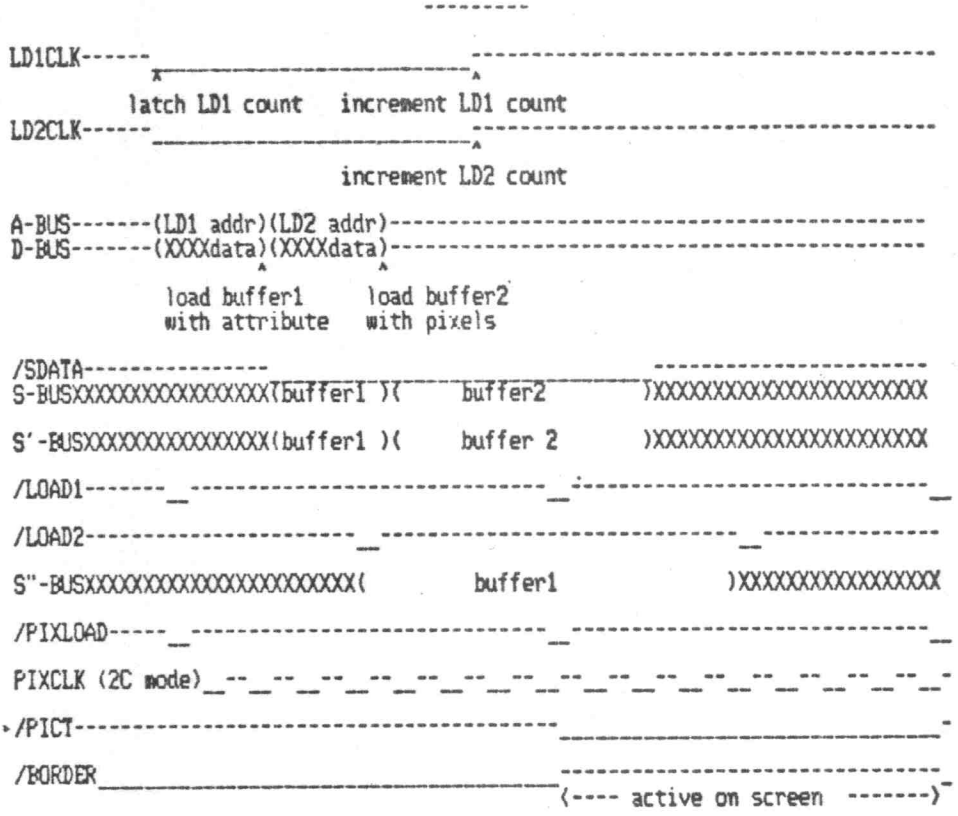
A TYPICAL DISPLAY (ACTIVE FROM COLUMNS 31 TO 32)



LPIXEL MODE


LD1CLK
latch LD1 count
increment LD1 count
A-BUS (LD1 addr) (LD1 addr)
D-BUS (XXXXdata) (XXXXdata)
load buffer1 with pixels
load buffer2 with same pixels
/SDATA
S-BUS (buffer1) (buffer2)
S'-BUS (buffer1) (buffer 2)
/LOAD1
/PIXLOAD
PIXCLK (2C mode)
PIXCLK (4C mode)
PIXCLK (16C mode)
PIXCLK (256C mode)
/PICT
/BORDER
(---- active on screen -------)

ATTR MODE


LD1CLK
latch LD1 count
increment LD1 count
LD2CLK
increment LD2 count
A-BUS (LD1 addr)(LD2 addr)
D-BUS (XXXXdata)(XXXXdata)
load buffer1 with attribute
load buffer2 with pixels
/SDATA
S-BUS (buffer1)(buffer2)
S'-BUS (buffer1)(buffer 2)
/LOAD1
/LOAD2
S"-BUS (buffer1)
/PIXLOAD
PIXCLK (2C mode)
/PICT
/BORDER
(---- active on screen -------)

CHARACTER MODE